MUCTPI high-speed serial link testing

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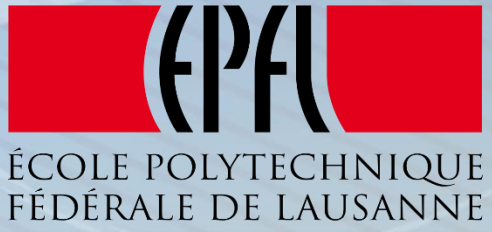


Outline

- Serial link testing
  - IBERT Firmware
  - Loopback and MUCTPI lab tests
  - High-speed oscilloscope measurements
- TTC recovery
- SL to MUCTPI data transfer tests
- TGC SL integration tests
- Power dissipation
- Conclusions & next steps

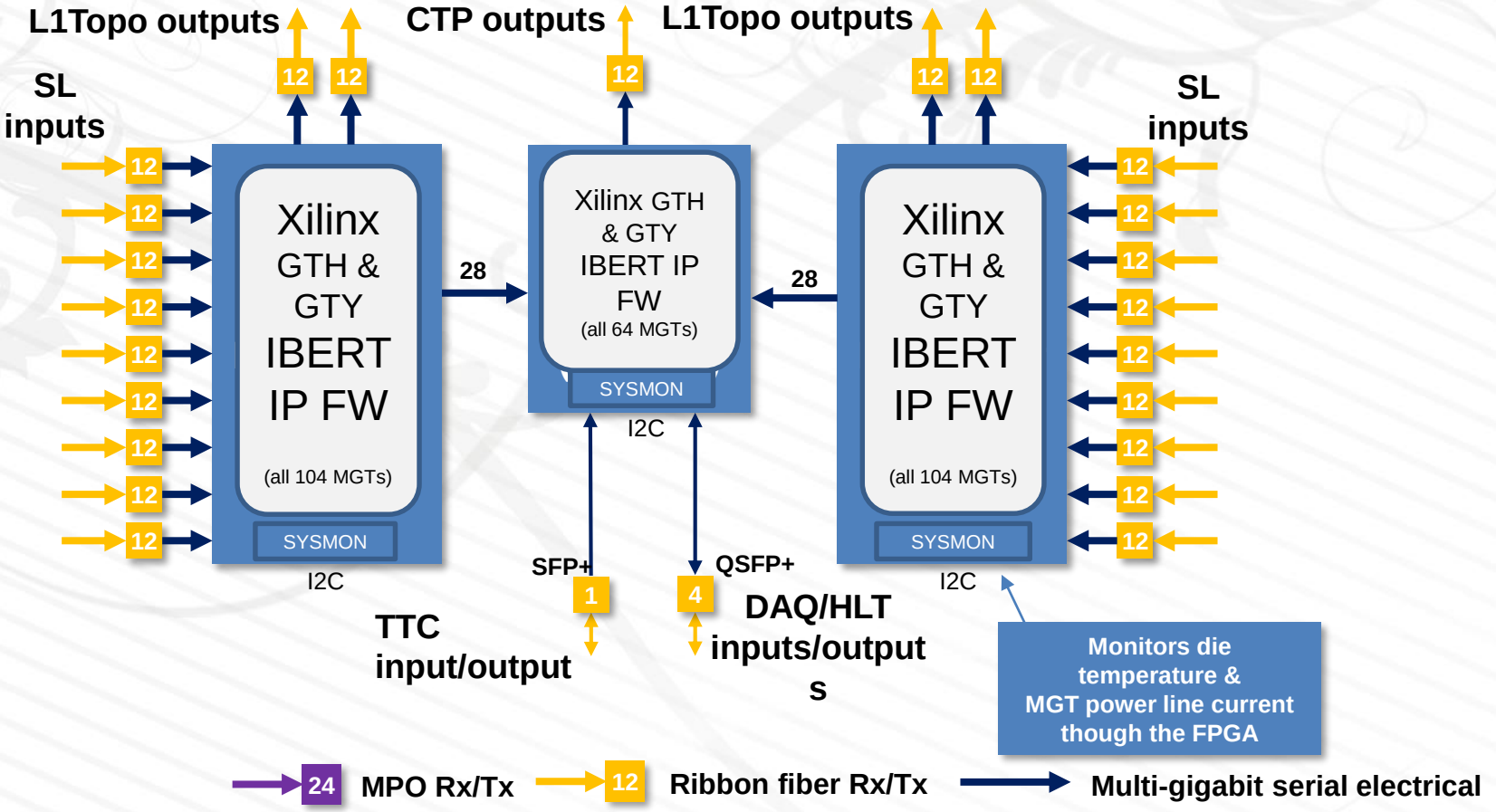
Serial link testing - IBERT Firmware

3 FW versions for testing ~270 links concurrently running at:

6.4 Gbps : Phase-I

9.6 Gbps: Phase-II

12.8 Gbps : Stress test



Serial link testing

MUCTPI partially populated module

L1Topo outputs

CTP outputs

L1Topo outputs

SL inputs

SL inputs

Xilinx GTH & GTY IBERT IP FW

all 104 TX/RX

SYSMON

I2C

28

Xilinx GTH & GTY IBERT IP FW (all 64)

SYSMON

I2C

28

Xilinx GTH & GTY IBERT IP FW

all 104 TX/RX

SYSMON

I2C

SFP+

QSFP+

TTC input/output

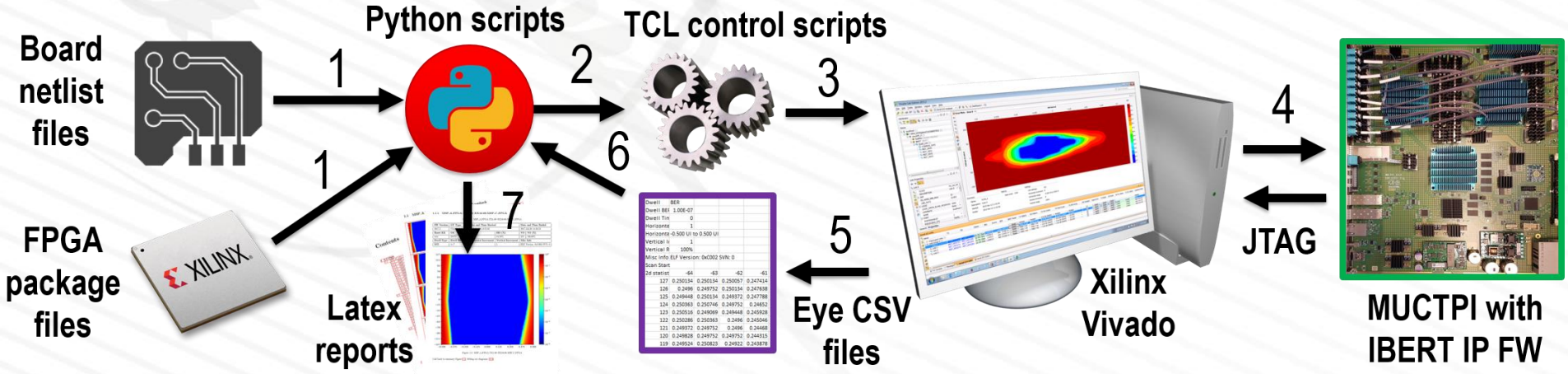
DAQ/HLT inputs/outputs

Monitors die temperature

Loopback examples — 24 MPO Rx/Tx — 12 Ribbon fiber Rx/Tx — Multi-gigabit serial electrical

Serial link testing - Software

- High number of links (330+ MGTs, ~270 links)
- Swap between MGT channels and polarity inversions during PCB layout
- Software: Python scripts were generated to:
  - **Extract interconnectivity information from the back-annoted board design**
  - **Automate the interconnection between links in Vivado**
  - **Polarity configuration**
  - **Test running in Vivado**
  - **Report generation for all the links running at 6.4, 9.6, and 12.8 Gb/s**



Serial link testing – Results – 6.4 Gb/s

Contents

1.1 MSP_A TX1 MSP_C RX16 Minipod Loopback

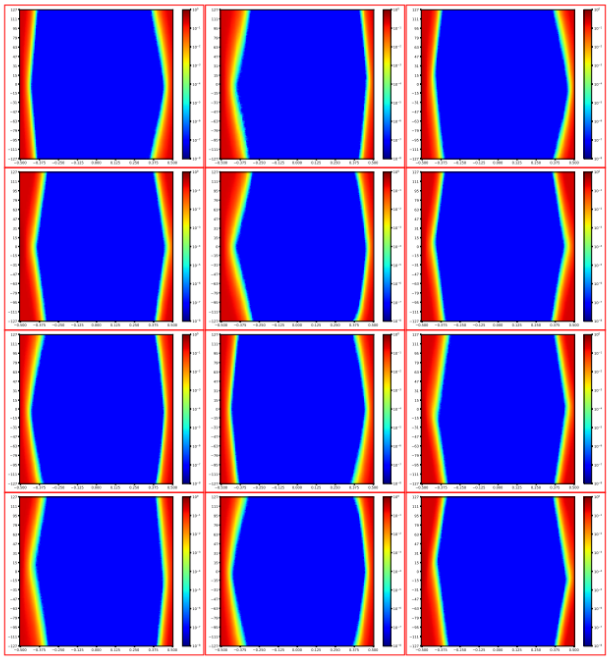


Figure 1.1: MSP_A TX1 MSP_C RX16 Minipod Loopback

A cross-reference to Figure 1.1. Sibling eye diagrams: 12.8.
Next summary Figure 1.14.

1.1.1 MSP_A_FPGA-TX1-00–RX16-00-MSP_C_FPGA

Table 1.1: MSP_A_FPGA-TX1-00–RX16-00-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended
2017.2	UltraScale GTH	2017-Jul-26 14:55:42		2017-Jul-26 14:56:53
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	25873	109	84.50%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

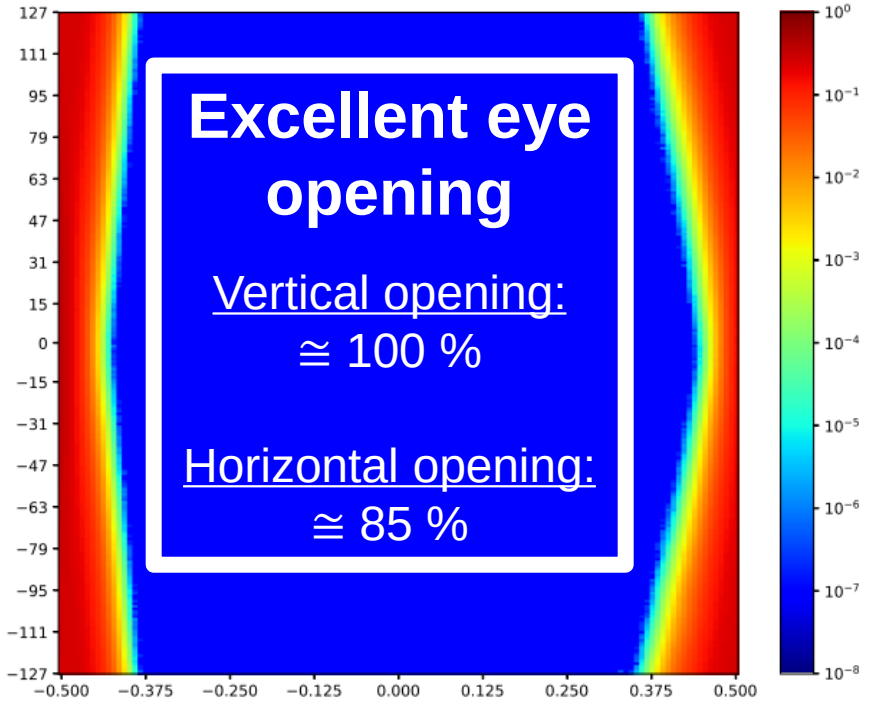
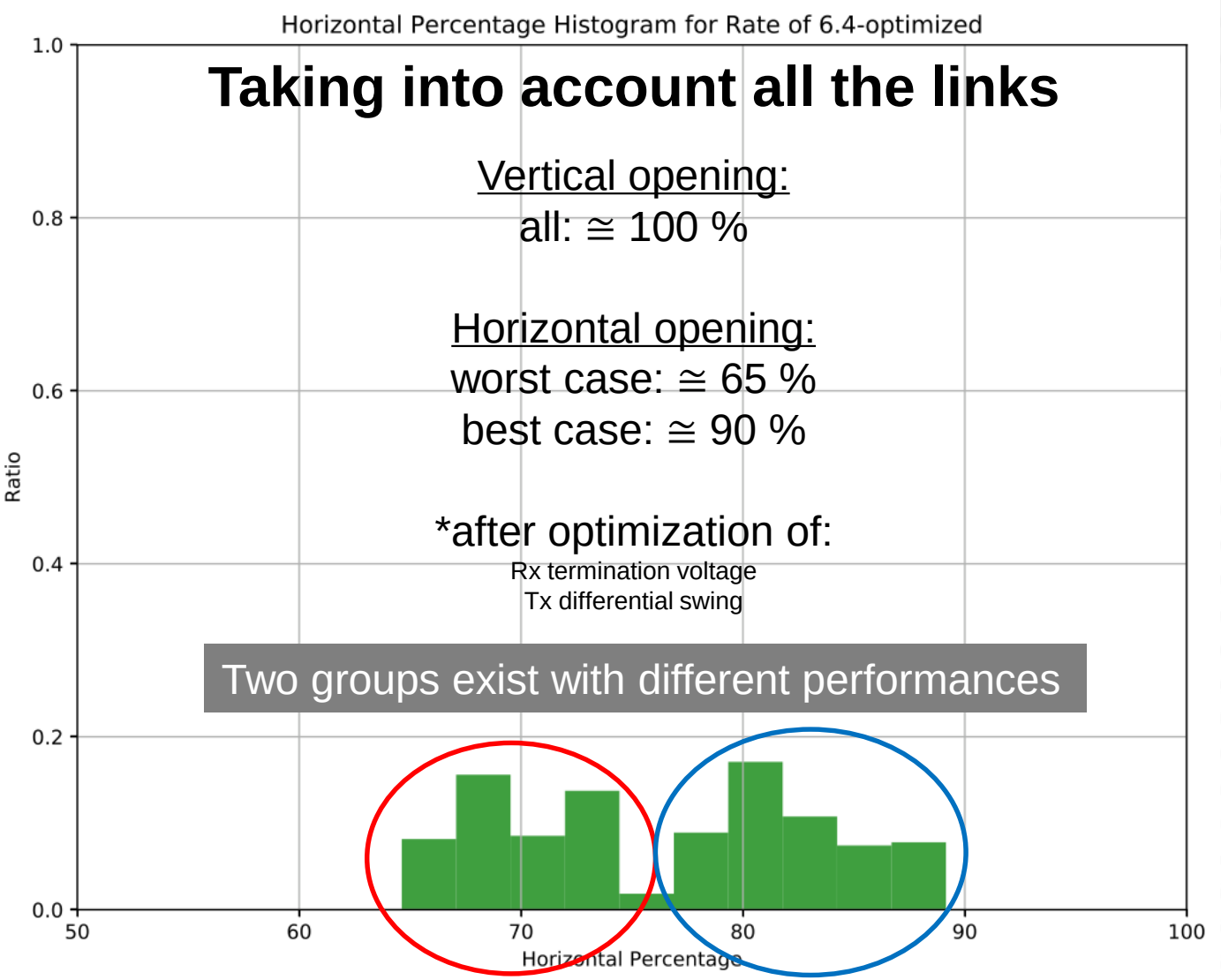


Figure 1.2: MSP_A_FPGA-TX1-00–RX16-00-MSP_C_FPGA

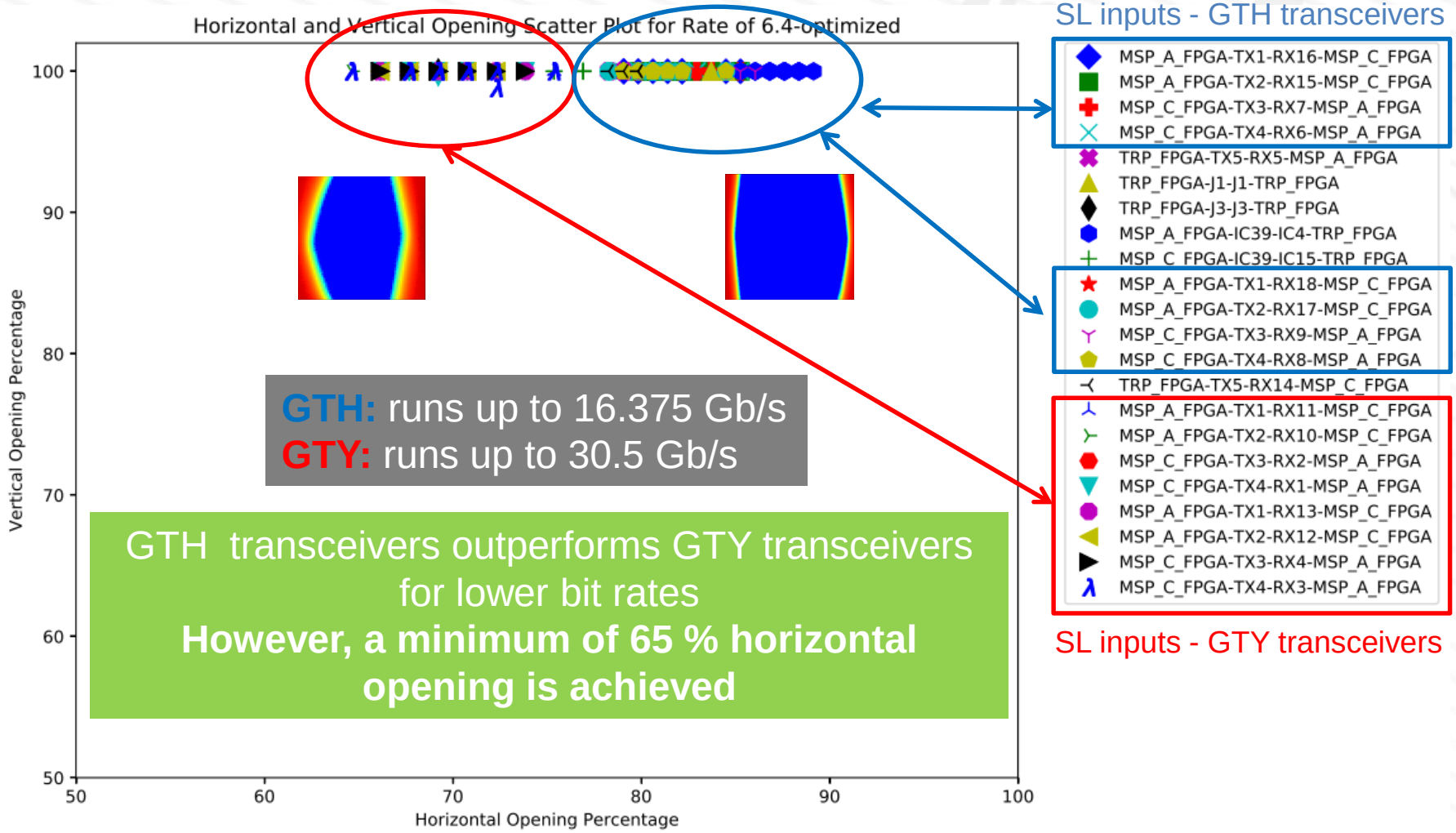
Call back to summary Figure 1.1. Sibling eye diagrams: 12.8.

269 RXs connected x 3 rates ≅ 800 eye diagrams measured

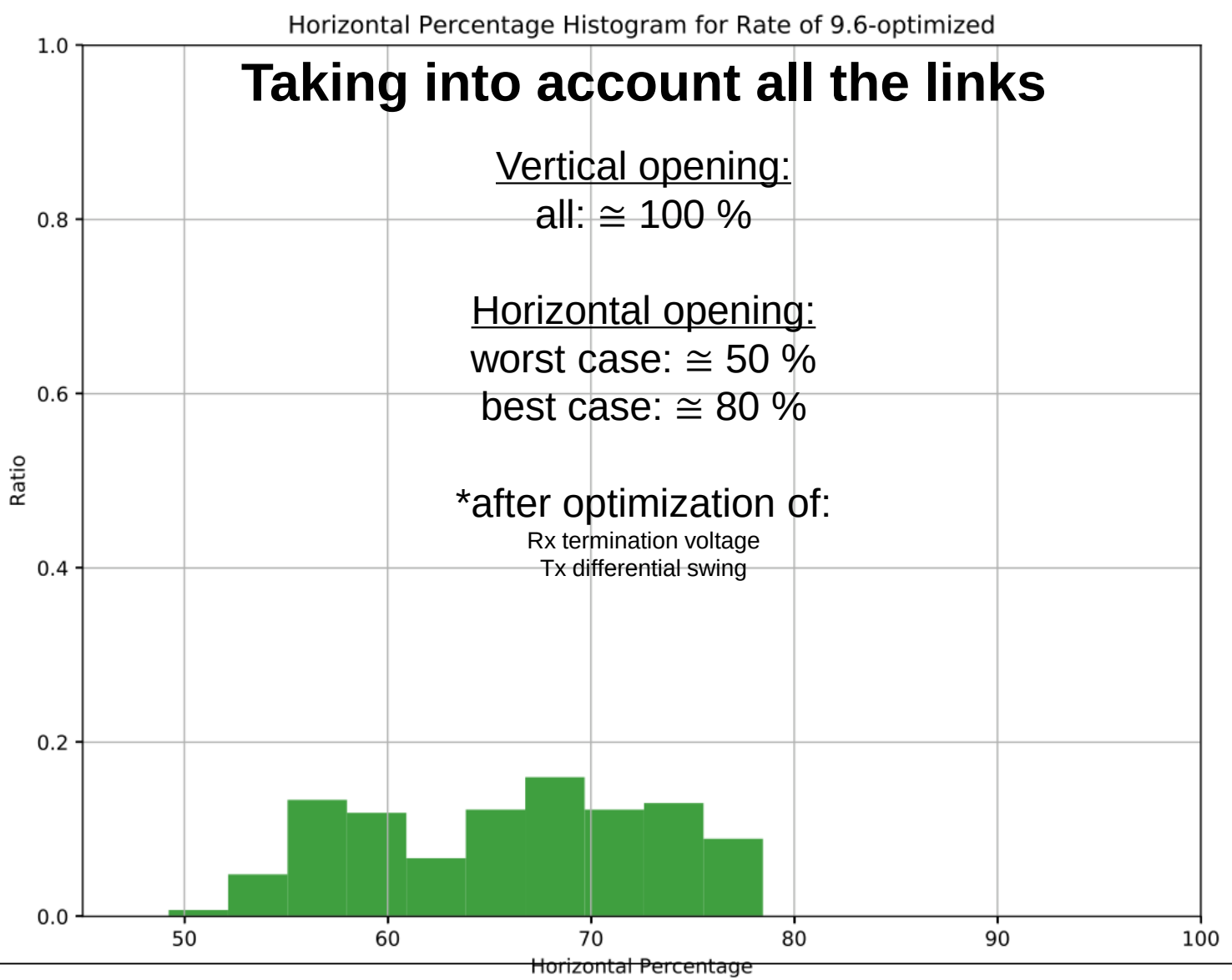
Serial link testing – Results 6.4 Gb/s



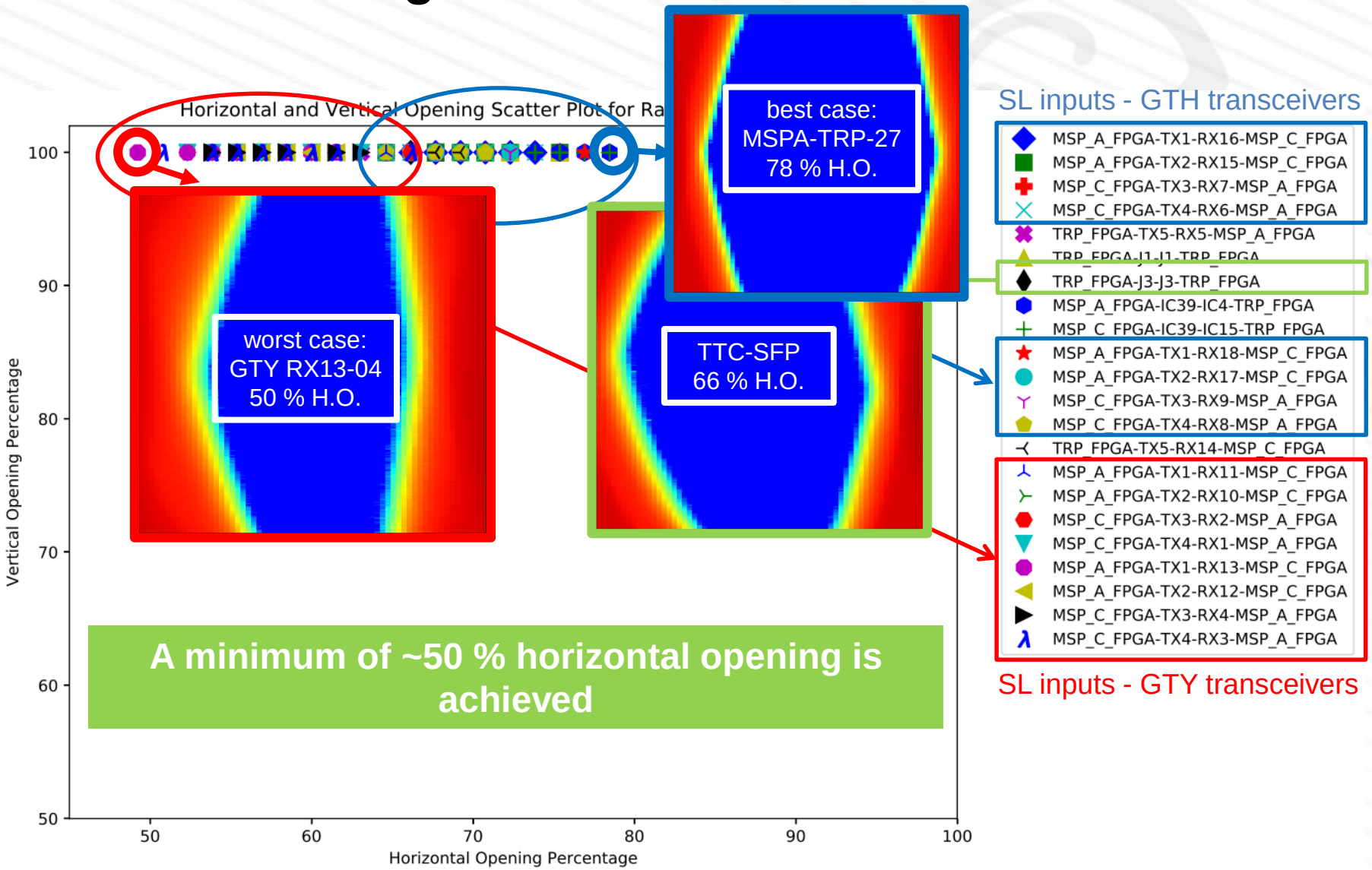
Serial link testing – Results 6.4 Gb/s



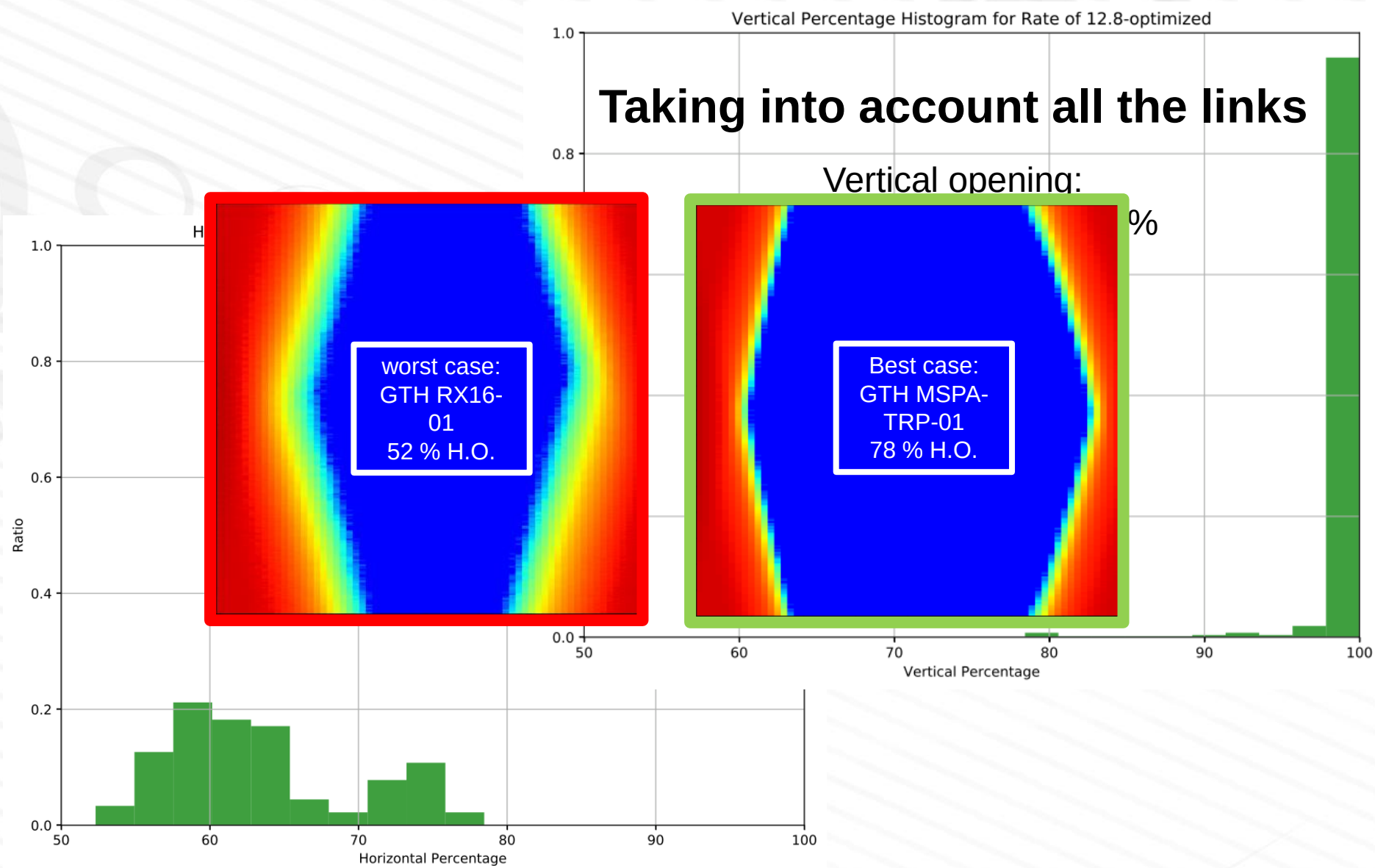
Serial link testing – Results 9.6 Gb/s



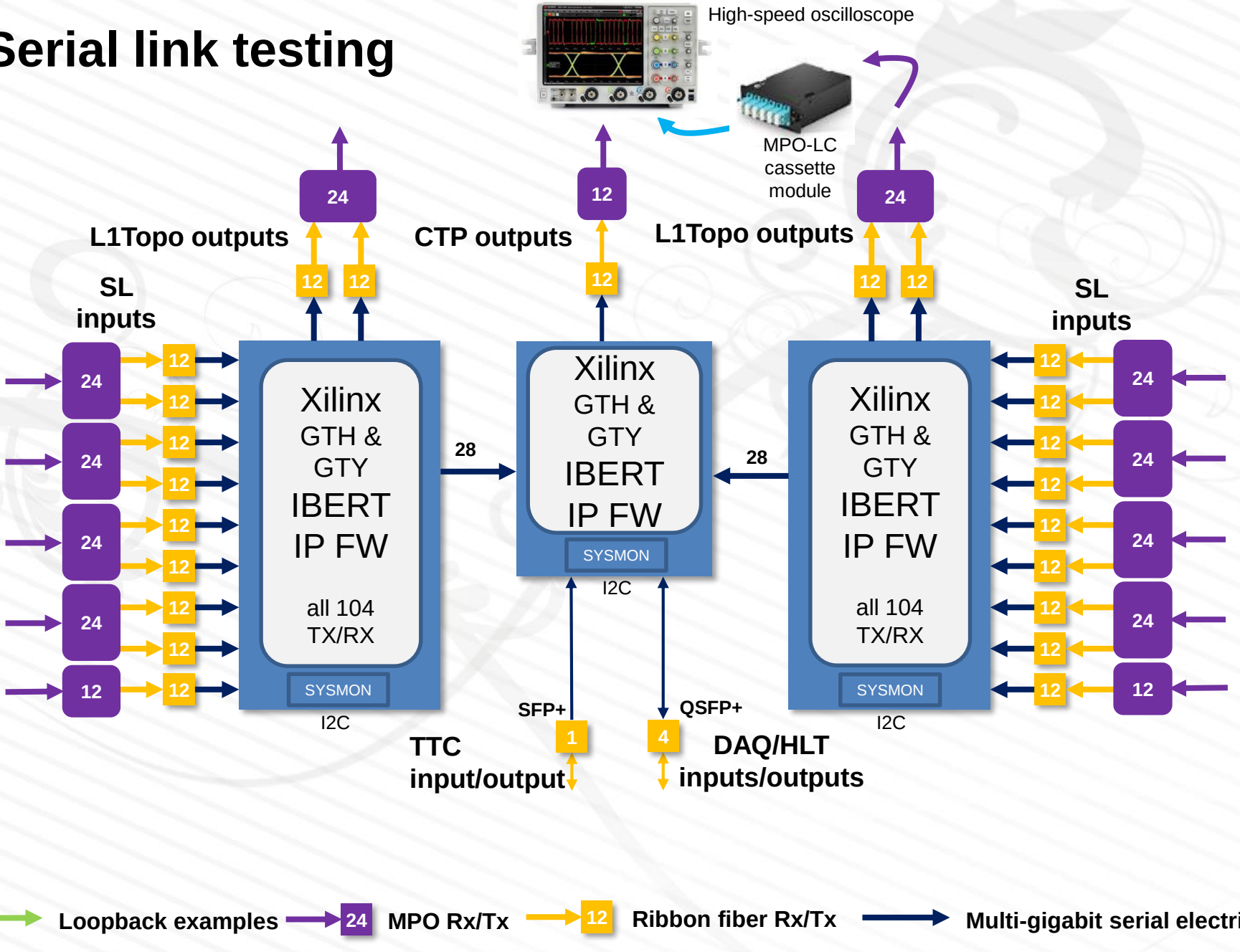
Serial link testing – Results 9.6 Gb/s



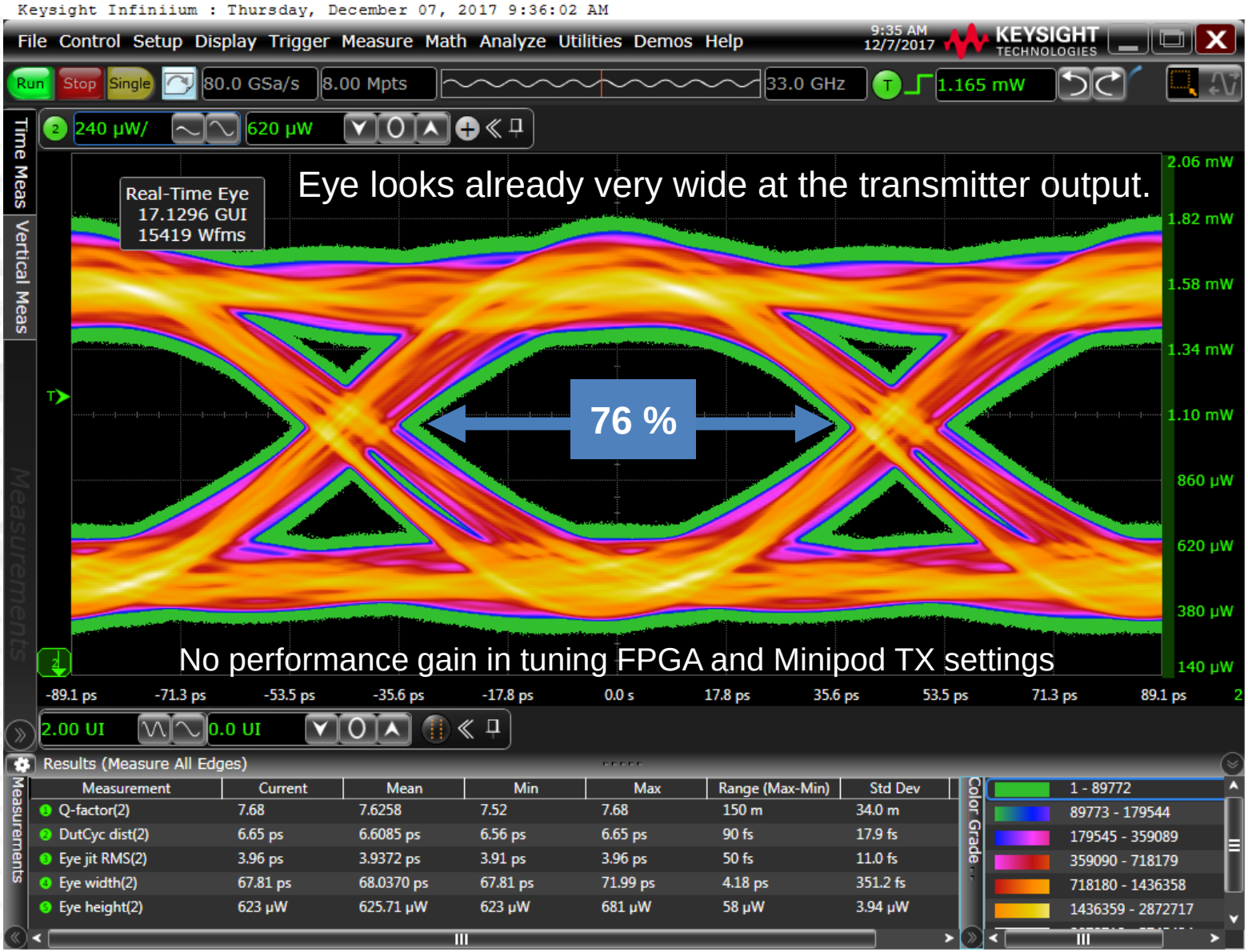
Serial link testing – Results 12.8 Gb/s



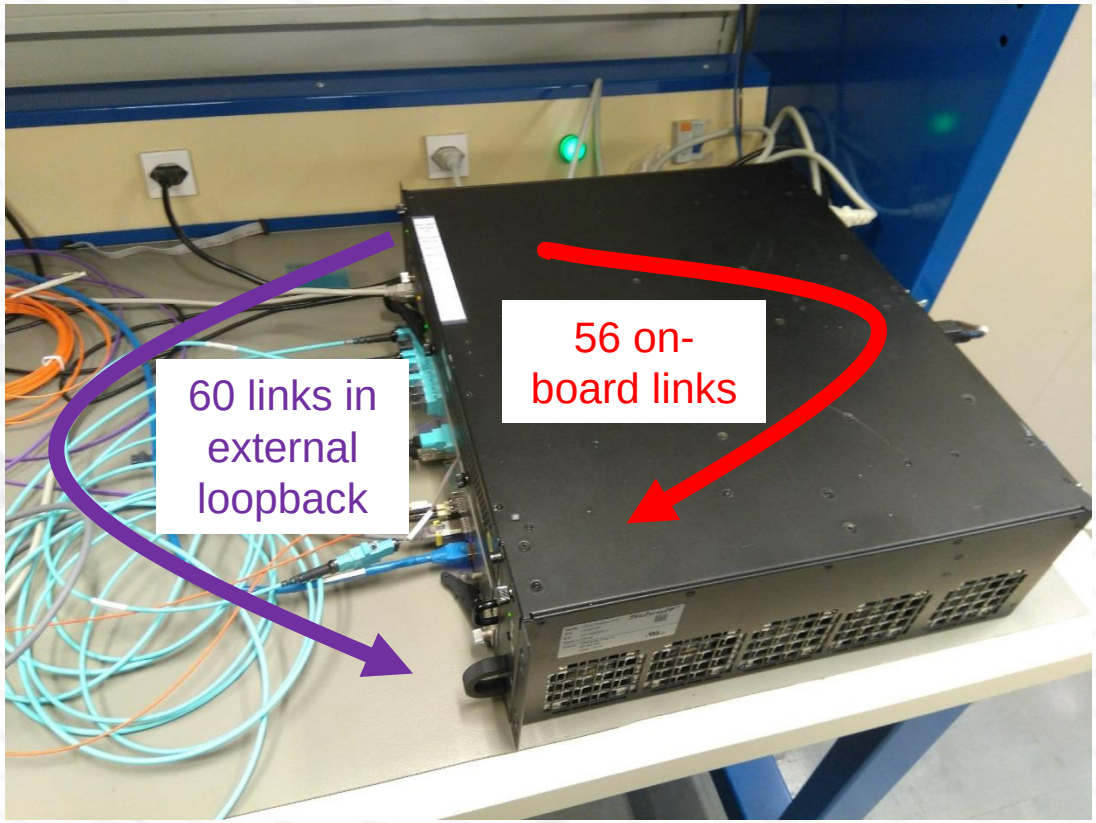
Serial link testing



Serial link testing – L1Topo out @ 11.2 Gb/s



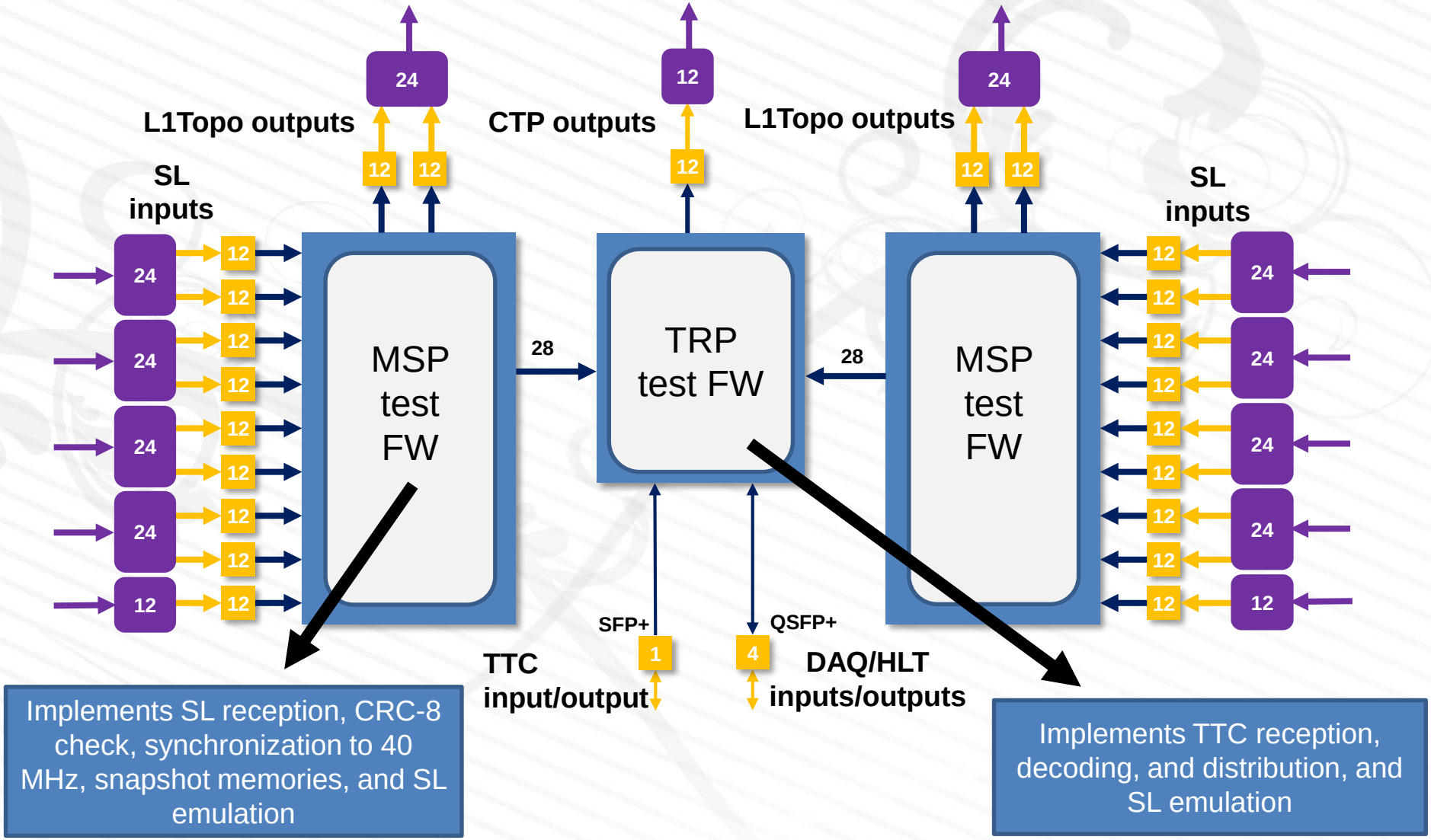
Serial link testing – Long term results



10 days error-free PRBS-31 data transfer over 116 serial links running at 12.8 Gb/s, BER < 10^{-15} (95 % confidence level)

The current MUCTPI prototype can send/receive data in 6.4 Gb/s, 9.6 Gb/s and 12.8 Gb/s

Serial link testing – SL & TTC reception Firmware



MUCTPI Firmware– TGC SL Data format

Muon Trigger Sector Logic - MUCTPI Test Pattern Proposal																
16-bit word	Upper-byte								Lower-byte							
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	Muon Candidate 1															
1	Muon Candidate 2															
2	Muon Candidate 3															
3	Muon Candidate 4															
4	Global flags								BCID							
5	CRC-8								0xFD (K29.7)							
6	0xC5 (D5.6)								0xBC (K28.5)							
7	0xC5 (D5.6)								0xC5 (D5.6)							

Observations:

Payload

Used for frame alignment

Used for word alignment

1) 8b/10b encoding is enabled

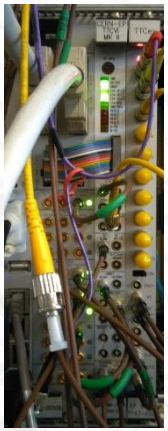
2) 16-bit word 0 is sent first

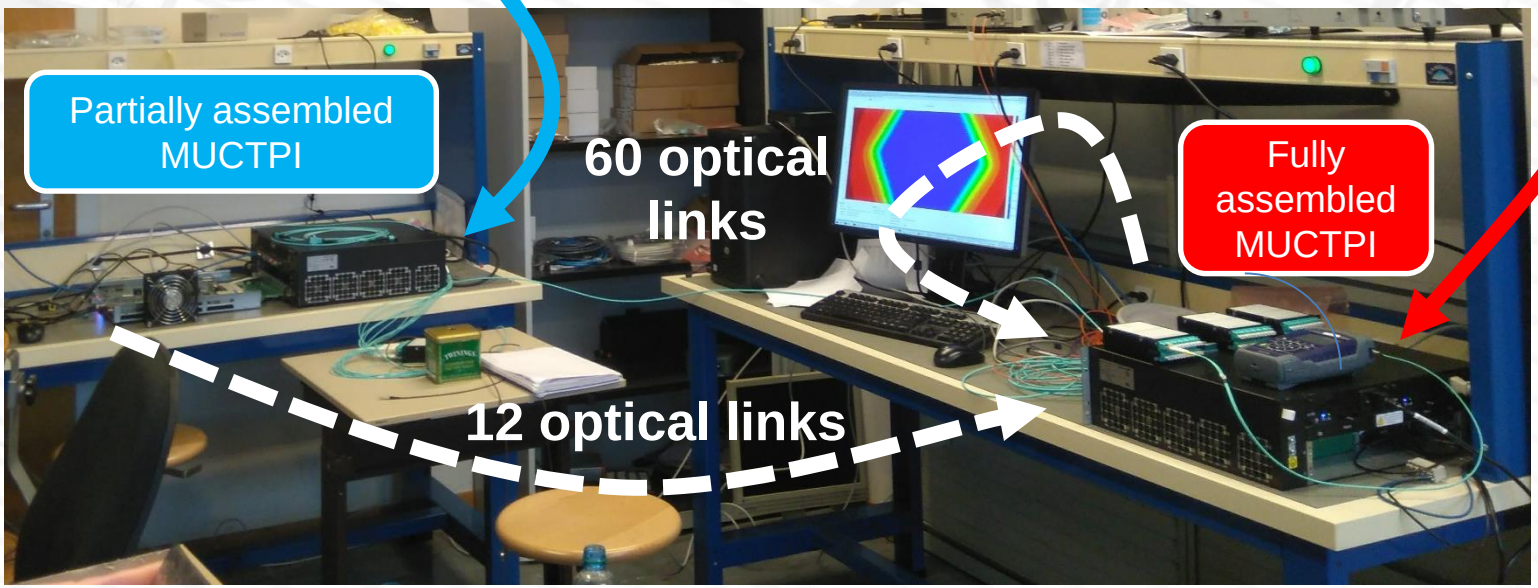
3) LSB bit is sent first (default for Xilinx)

	K character enabled
	K character disabled

SL Reception Firmware Lab Test

LTP + TTC vi + TTC ex



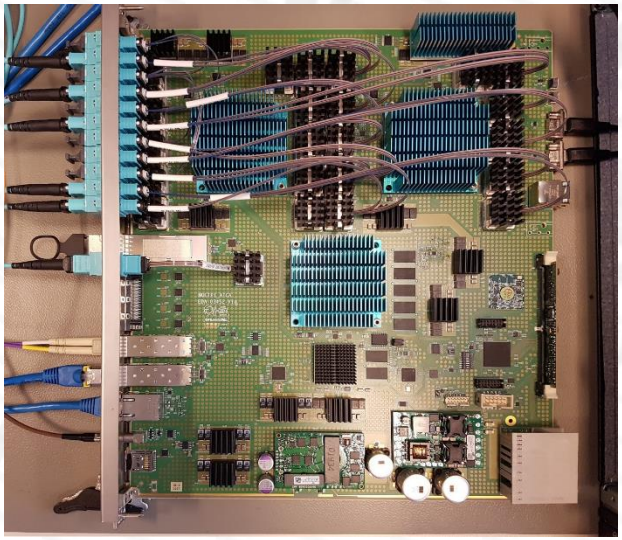


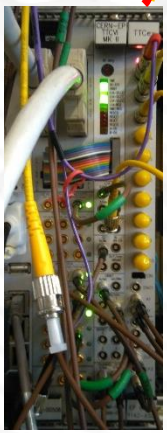
Data transfer using two MUCTPI modules connected to two TTC connections.
72 links in total. Latency constant. No errors in an overnight run.

TGC integration test

TGC SL
prototype

12 x





LTP
+
TTC
vi
+
TTC
ex

TGC integration test – BER test

- Connection from 12 TGC SL channels to MUCTPI GTH and GTY channels
- BER overnight test without errors
- Horizontal opening > 65 %
  - The same as seen in the loopback tests

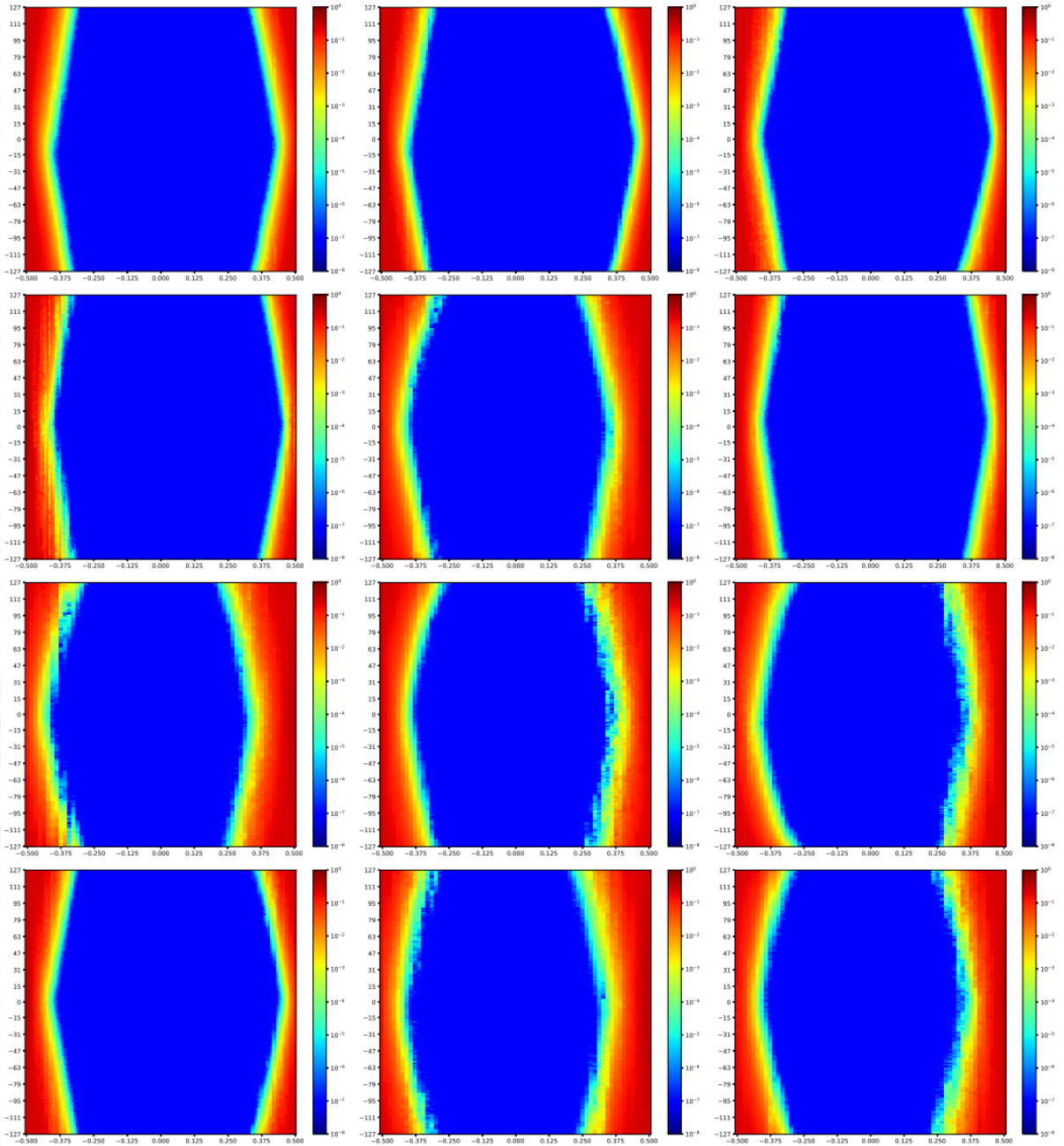


Figure shows the eye diagram of the optical data transfer of a PRBS-31 pattern from TGC SL channels 0-11 to the MUCTPI. The eye opening is very good. Horizontal opening ranging from 66% to 81%.

TGC integration test

- Data from all 12 channels received and synchronized to the bunch clock with no CRC errors.
- Latency from SL 40 MHz to MUCTPI 40 MHz clock domain ≈ 4.5 BCK period
  - The same as seen in the CTP lab
- Snapshot memory used to record data from 4K BCs. Data was checked by software. No errors.

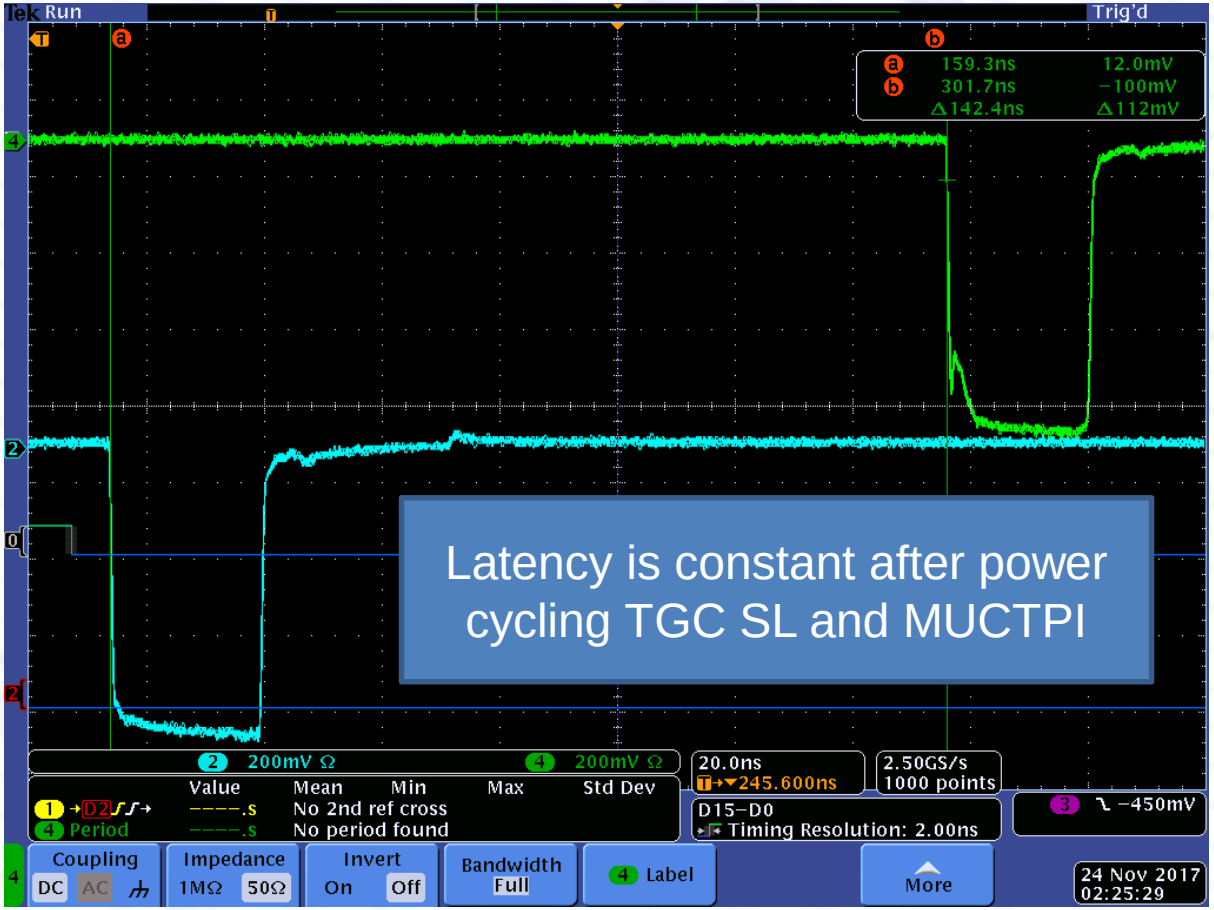
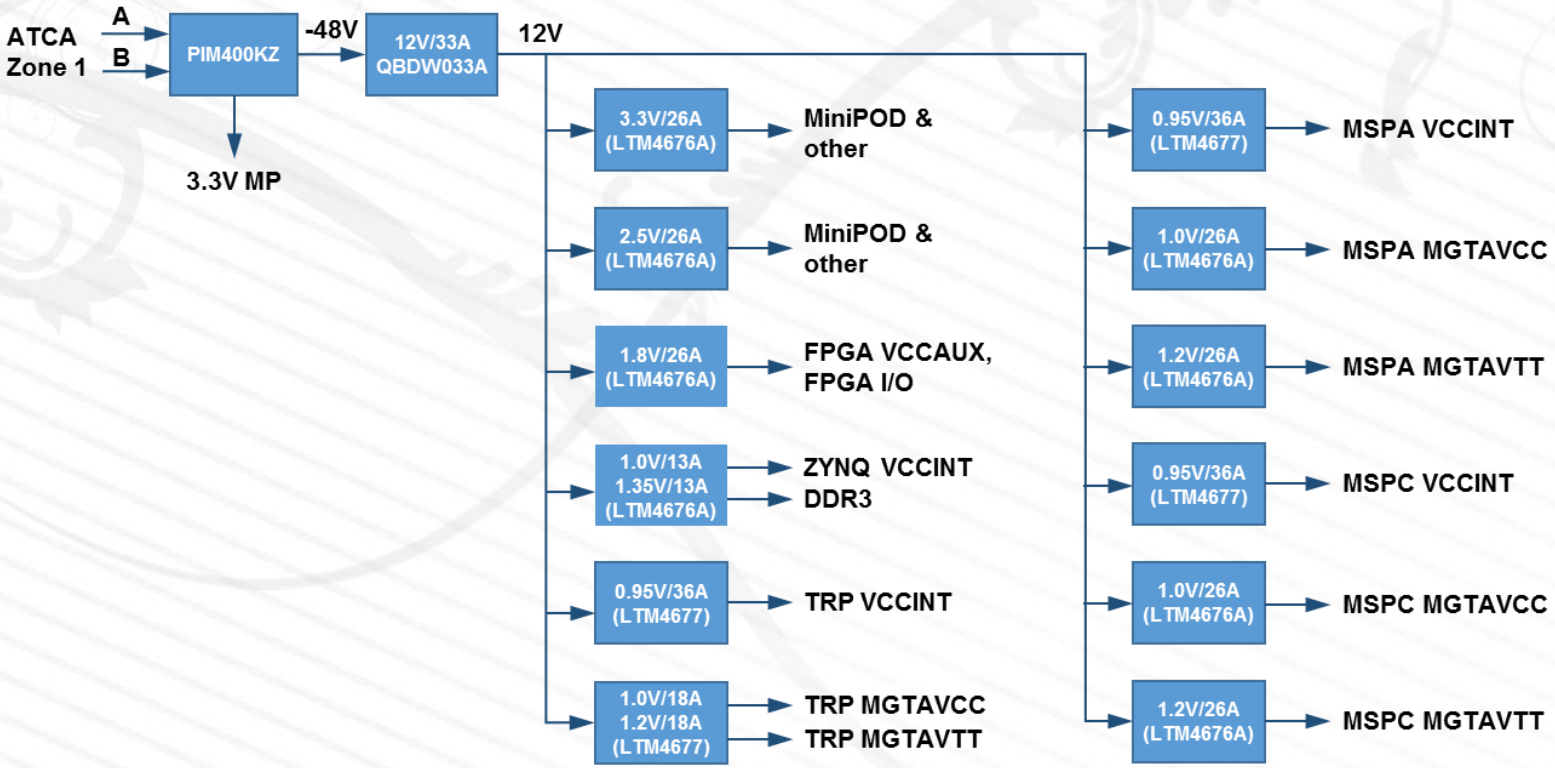


Figure shows the oscilloscope acquisition waveform used to measure the latency between the sector logic module prototype to the MUCTPI demonstrator. The sector logic module asserts a flag (oscilloscope channel 2) when the 128-bit word associated to BCID 0 is sent in the 40-MHz clock domain logic. When the same 128-bit word is received, the MUCTPI asserts a second flag (oscilloscope channel 4). 4 ns has to be deducted from the measured value to compensate the combinatorial delay in the TRP FPGA. In addition, 5m x 5 ns/m = 25 ns should be deducted from the measured value, for the latency in the optical fibres. Therefore the latency is ≈ 113 ns, which corresponds to ≈ 4.5 BCK period.

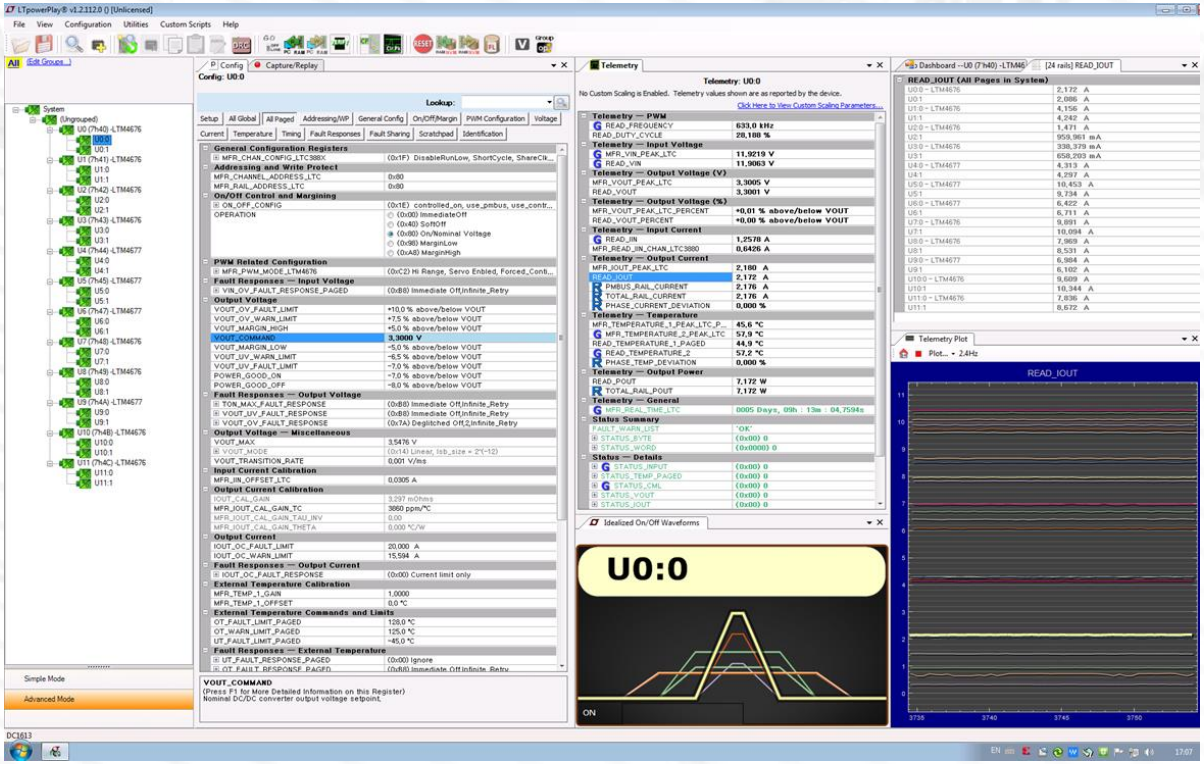
Power supply design

- **2-stage power conversion:**
  - **ATCA power entry module & -48V/12V isolated DC/DC converter (400W)**
  - **Point-of-Load (POL) converters generate all payload voltages from 12V**
  - **Separate POL converters for the core and MGT supplies of each FPGA**
    => 12 POL DC/DC modules in total



Power supply design

- **Fully integrated DC/DC modules from Linear Technology**
  - **LTM4676A (2 x 13A) and LTM4677 (2 x 18A), dual output**
  - **PMBus interface for configuration and monitoring**
  - **Programmable power sequencing**
  - **GUI for programming (on-chip EEPROM) and monitoring**



Power dissipation

- SL reception firmware (MGTs running in the rate we need, core logic incomplete)
- IBERT 12.8 Gb/s (all MGTs running at 12.8 Gb/s)

	MSP A			MSP C			TRP			Global				
	MGTAVCC	MGTAVTT	VCCINT	MGTAVCC	MGTAVTT	VCCINT	MGTAVCC	MGTAVTT	VCCINT	1V0	1V35	1V8	2V5	3V3
Device limit	26.00 A	26.00 A	36.00 A	26.00 A	26.00 A	36.00 A	13.00 A	13.00 A	36.00 A	13.00 A	13.00 A	26.00 A	26.00 A	26.00 A
Test FW	11.48 A	14.98 A	8.44 A	11.60 A	14.94 A	8.31 A	2.18 A	1.34 A	8.31 A	0.87 A	0.73 A	2.76 A	6.68 A	3.89 A
	44.14%	57.60%	23.45%	44.62%	57.45%	23.09%	16.74%	10.32%	23.09%	6.68%	5.60%	10.62%	25.68%	14.97%
IBERT 12.8 Gb/s	16.21 A	20.00 A	12.51 A	16.16 A	19.92 A	12.31 A	10.42 A	9.72 A	12.31 A	0.75 A	0.34 A	2.41 A	7.15 A	3.90 A
	62.35%	76.92%	34.74%	62.14%	76.62%	34.18%	80.17%	74.76%	34.18%	5.73%	2.61%	9.27%	27.49%	15.01%

- Test FW requires less than 60 % of power modules maximum current for all cases
- IBERT FW worst case power consumption is 80 % (running in 12.8 Gb/s, we actually are going to run it slower)
- The total power consumption is 210 W (~50% ATCA limit) using the 12.8 Gb/s IBERT FW)

	MSP A				MSP C			
	FPGA	MGTAVCC	MGTAVTT	VCCINT	FPGA	MGTAVCC	MGTAVTT	VCCINT
Test FW	50.00 °C	60.40 °C	59.50 °C	56.40 °C	50.00 °C	54.90 °C	61.90 °C	55.80 °C
IBERT 12.8 Gb/s	60.00 °C	69.00 °C	67.80 °C	61.40 °C	60.00 °C	61.40 °C	70.80 °C	64.50 °C

	MSP TRP				Global				
	FPGA	MGTAVCC	MGTAVTT	VCCINT	1V0	1V35	1V8	2V5	3V3
Test FW	34.00 °C	50.40 °C	50.40 °C	51.80 °C	49.70 °C	49.70 °C	52.90 °C	55.80 °C	53.50 °C
IBERT 12.8 Gb/s	57.00 °C	59.70 °C	59.70 °C	57.80 °C	52.40 °C	52.40 °C	55.30 °C	57.40 °C	54.80 °C

The temperature values applies to the integrated power control IC based on the LTC®3880. The LTC®3880 can operate up to 150 °C.

- All the FPGAs temperature < 60 °C
- Temperature in the power IC controller < 71°C for all cases. Device can operate up to 150 °C

Conclusions

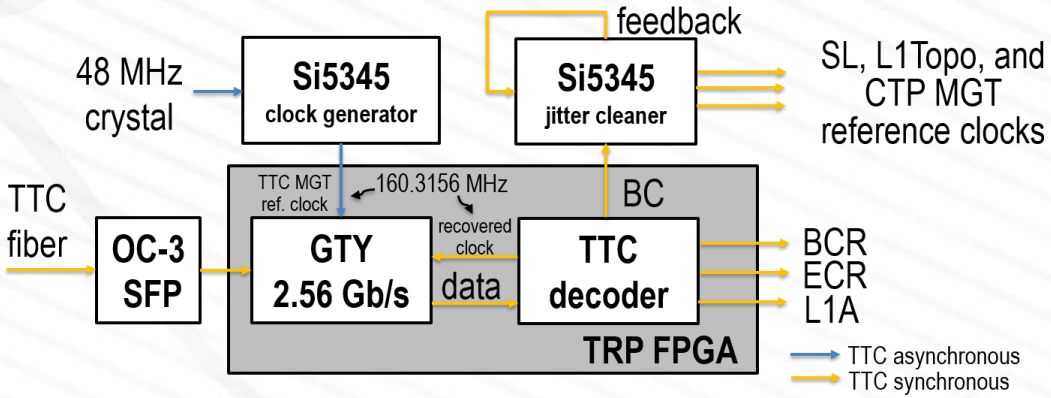
- SL, TTC, and power supply MUCTPI prototype tested successfully
  - SL: Eye diagrams are wide open
    - 6.4 Gb/s: no errors even using 7 dB optical power attenuator
    - 12.8 Gb/s: error-free run over 10 days
  - SL & TTC reception FW is ready and tested with TGC prototype
  - SL & TTC reception constant latency demonstrated
  - Power supply system: works successfully with all links active

- Next steps:
  - Connection tests with RPC interface board
  - Functional/algorithm firmware development
  - Data format proposal to L1Topo

Backup slides

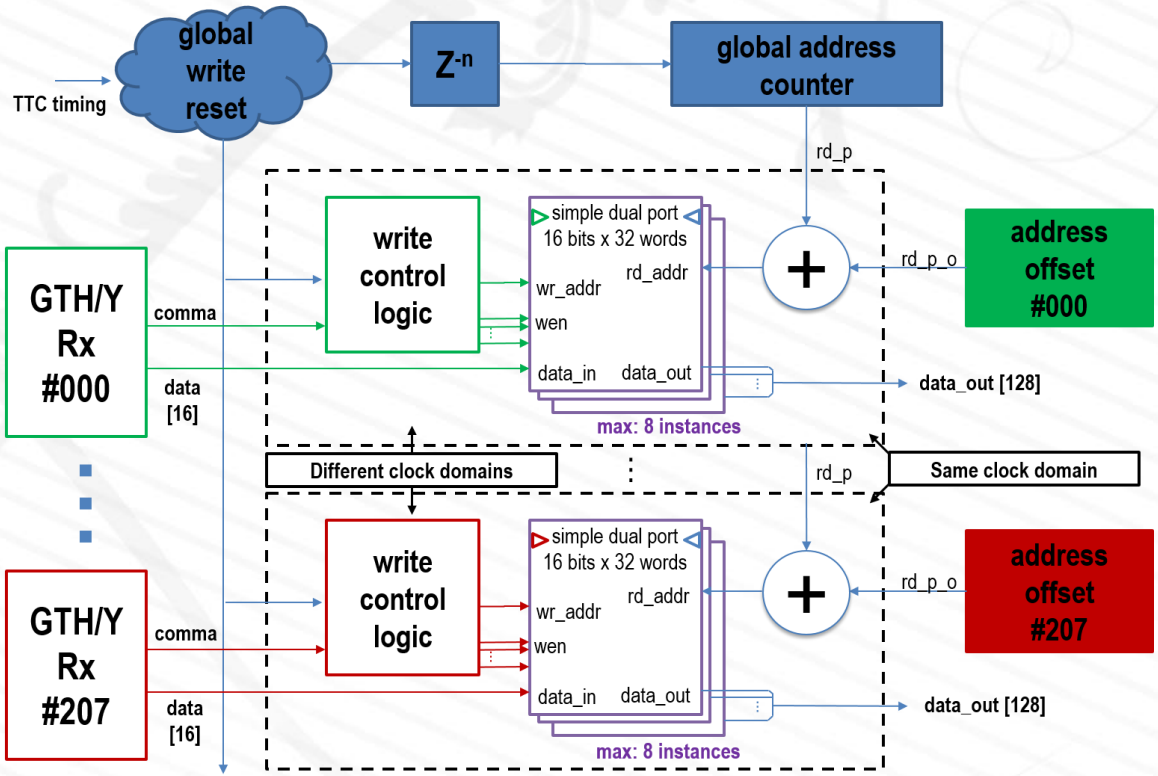
Timing, Trigger & Control (TTC) recovery

- Circuit based on external CDR ADN2814 will be used to recover the TTC
  - The same circuit as TTC FMC, widely used and tested at CMS
- An alternative was tested: General purpose transceiver and user logic to receive TTC (replaces TTC FMC)
  - OC-3 SFP transceiver module (optical → electrical transmission)
  - 2.56 Gb/s GTY oversamples 160 Mb/s TTC encoded signal
  - GTY outputs 160 MHz TTC recovered clock
  - User logic aligns recovered clock & data, decodes TTC, and generates 40 MHz
  - Jitter cleaner cleans TTC clock and generates required MGT reference clocks



SL input Synchronization & Alignment

- Has to compensate the input phase-skew
- Align the signals in multiples of the bunch-crossing period of 25 ns
- Write control logic detects BC frame boundaries
- Dual port memories transfer all 208 inputs from their respective clock domains into a single clock domain for combined data processing
- It can cope with phase variation of the received data and non-deterministic data transfer latency from FPGA transceivers by monitoring received data timing and setting logic delays in the write control logic
- Reduced version already tested with barrel and end-cap SL prototypes
- Complete version tested with 72 links running concurrently
- Will be used for connection tests with end-cap SL prototypes



MUCTPI demonstrator

- Custom double-width FMC card
- Designed to test FPGA family, on-chip MGTs, 12-channel ribbon fiber optics receiver and transmitter modules (MiniPOD), and clock circuitry
- Designed SL reception demonstration firmware
- Used successfully for connection tests with TGC and RPC sector logic modules