The ATLAS Level-1 Muon Topological Trigger Information for Run 2 of the LHC

Marcos Vinicius Silva Oliveira

Outline

- Introduction
- Level-1 muon trigger
- Feasibility tests
  - Development
  - Results
- MUCTPI firmware upgrade for Run 2
  - Development
  - Verification
- Integration tests
- Conclusions

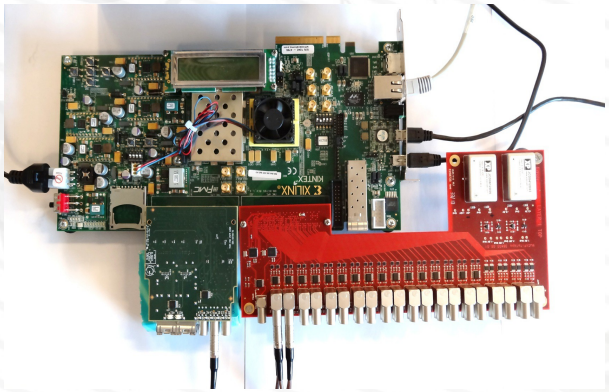
Introduction

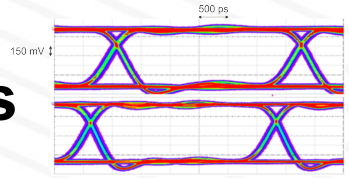
- **Modern HEP Experiments, such as the ATLAS experiment including the Muon trigger, require advanced electronic instrumentation systems, as the Muon-to-Central-Trigger-Processor Interface**
  - Process physics event data at high rates from thousands of channels
- **Such processing requires on-line filtering, also known as triggering**
  - It has to be fast. Therefore implemented in hardware
- **The digital processing in the MUCTPI is implemented using FPGA devices**
  - High processing capacity
  - Re-programmability (changing functionality by firmware upgrade)
- **The trigger efficiency for several physics processes can be improved using topological information in the Level-1 trigger system**
  - Firmware upgrade of the MUCTPI system in order to transmit muon topological information to L1Topo through the electrical trigger outputs

Overview

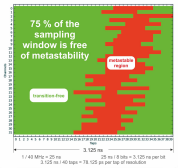
Feasibility tests

Development of an error rate test system



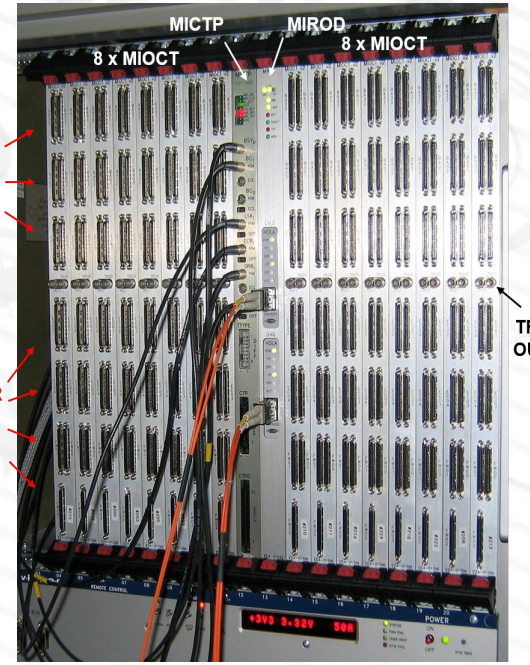


Maximum bit rate



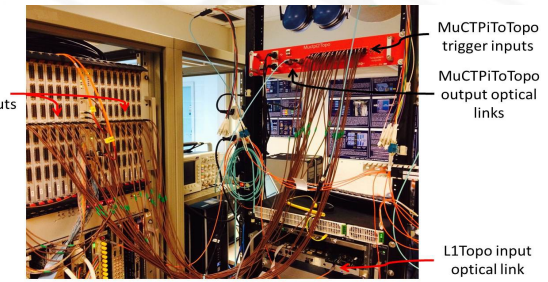
Topological information

MUCTPI firmware upgrade



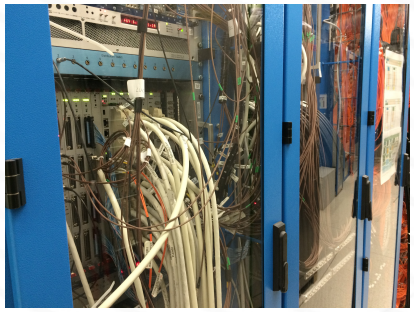
Integration tests in the lab

Verification of the upgraded MUCTPI system



Tests in USA15

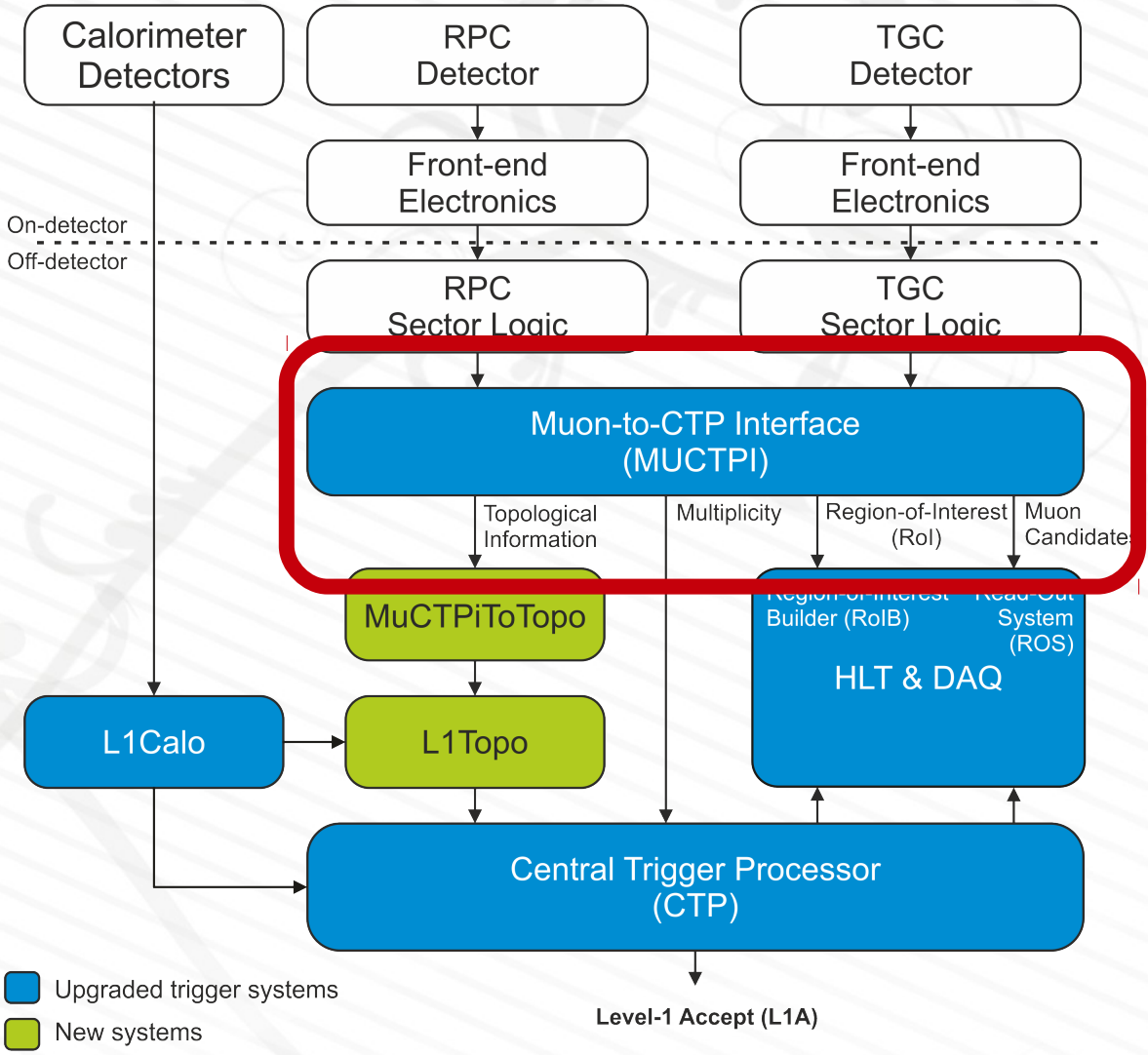
Test results in the lab



Level-1 muon trigger

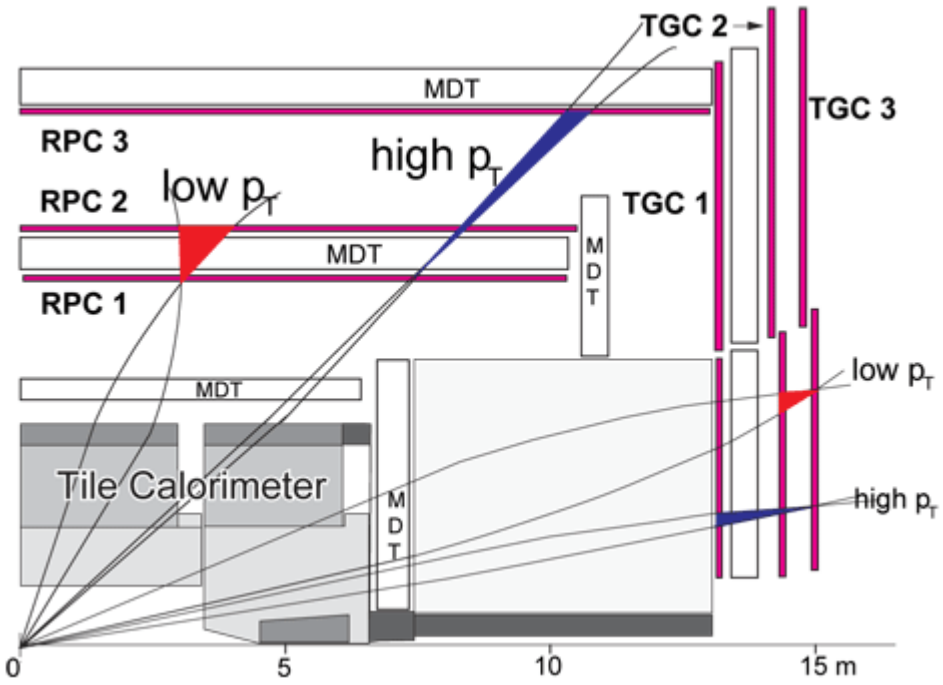
ATLAS Level-1 Trigger system

- Implemented with custom electronics.
- 40 MHz down to 75 kHz
- Decision based on multiplicity of trigger objects
- Topological information in Run 2 (2015-2018)
- The CTP will receive flags indicating the events that passed the topological trigger criteria



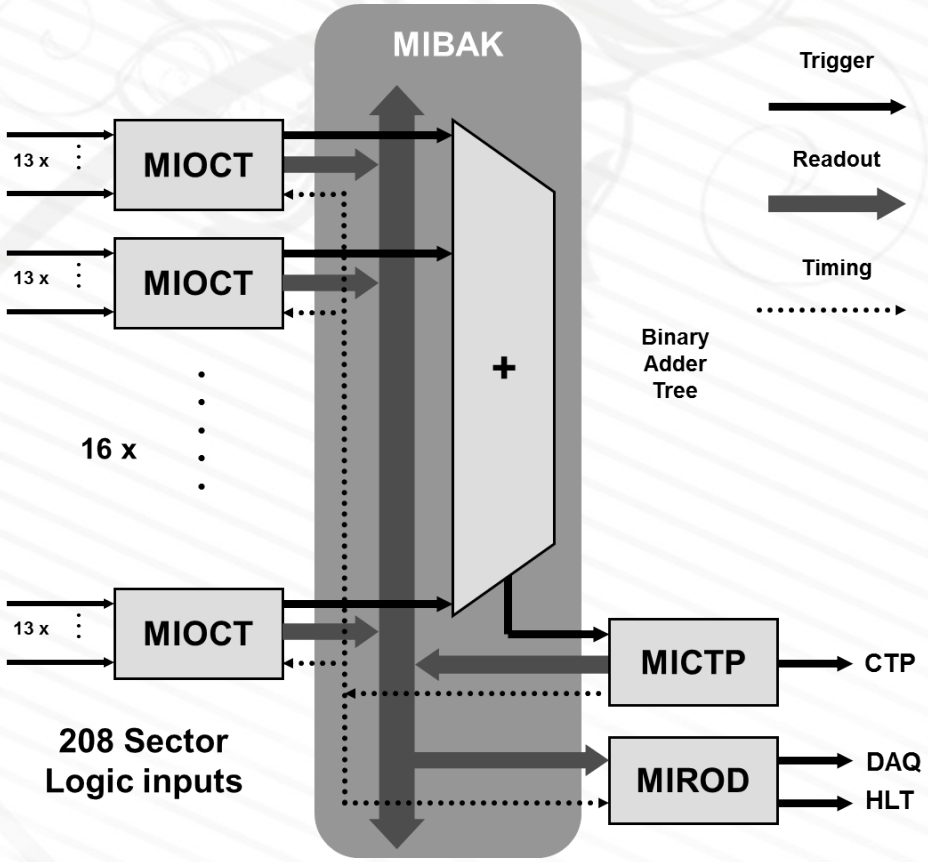
Muon trigger detectors

- Provides multiplicity and approximate energy range
- Fast response (15-25 ns)
- Resistive Plate Chambers (RPC) in the barrel
- Thin Gap Chambers (TGC) in the end-cap
- Momentum of muons is measured from magnetic deflection of muon tracks in the toroid magnets
- Smaller the bending, higher the momentum
- Trigger sector logic reconstructs muon tracks (three dimensionally) and sends to the MUCTPI



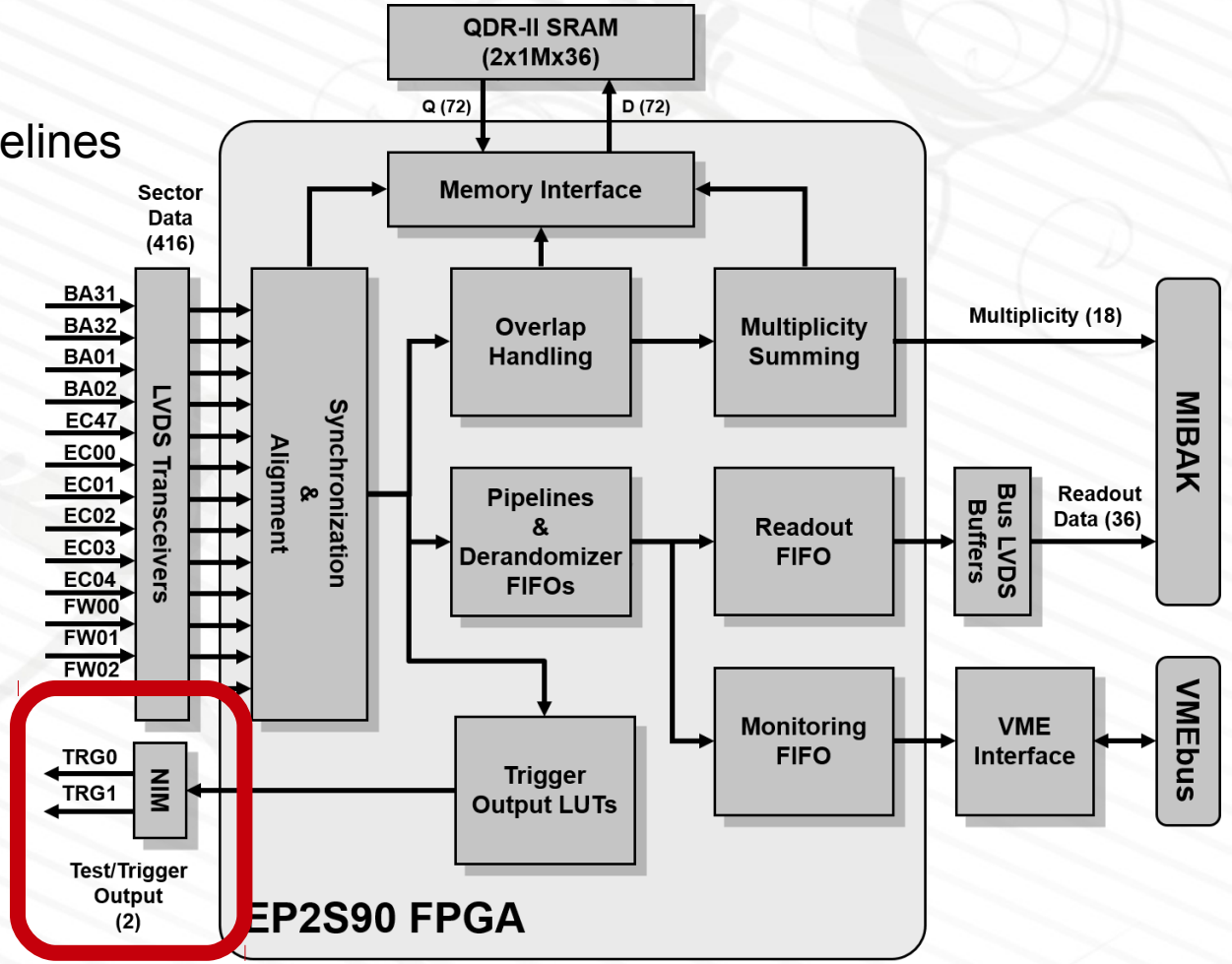
MUCTPI

- Calculates the total number of muon candidates for each of six pT thresholds avoiding double counting of muon candidate in overlap regions and sends to the CTP
- Consists of:
  - 16 octant modules (MIOCT): generates the local multiplicity, handles overlap, holds readout data and sends flags to CTP using the electrical trigger outputs
  - MIBAK: calculates total multiplicity, distributes timing and control signals and implements readout bus
  - MICTP: receives timing and forwards total multiplicity to the CTP
  - MIROD: collects readout data and the total multiplicity from the MICTP and sends them to HLT and DAQ systems



MIOCT

- Trigger and Readout in a single FPGA:
  - Synchronization using programmable length pipelines
  - Overlap handling using programmable LUTs
  - Holds readout data using FIFOs
  - SRAM memory used for validation and to capture sector input data
  - Sends trigger flags to the CTP **at the BC rate (40 Mbps)** using the electrical trigger outputs

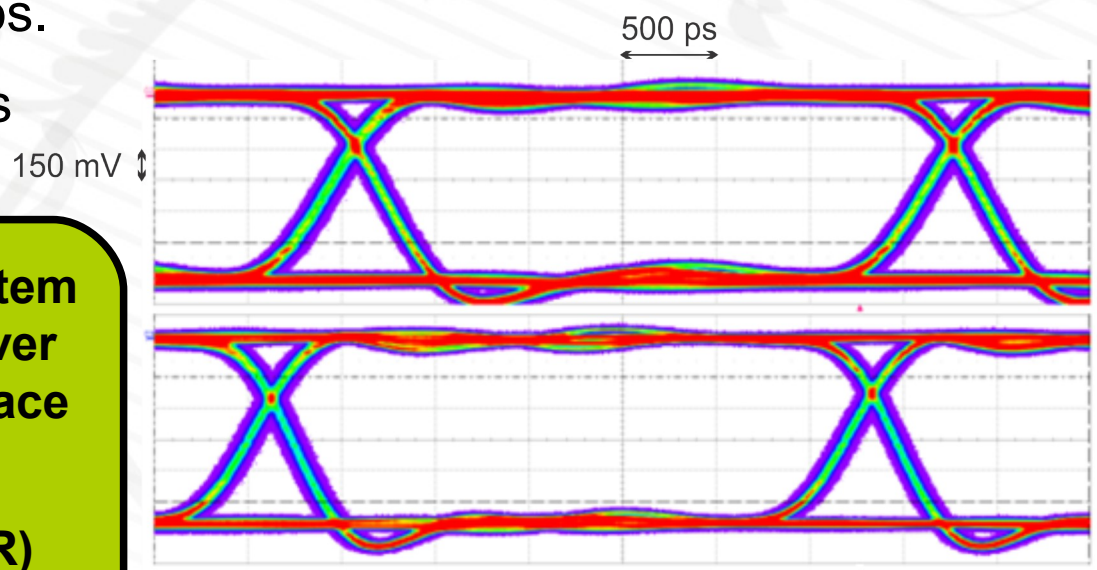


Feasibility Tests

Feasibility tests

Can these trigger outputs be used to transmit topological information to L1Topo?

- 40 Mbps is not sufficient even to send coarse muon topological information to L1Topo
- MIOCT firmware modification to send PRBS-31 data at 80 Mbps, 160 Mbps, 240 Mbps, and 320 Mbps.
- Open eye-diagram with outputs sending data at 320 Mbps

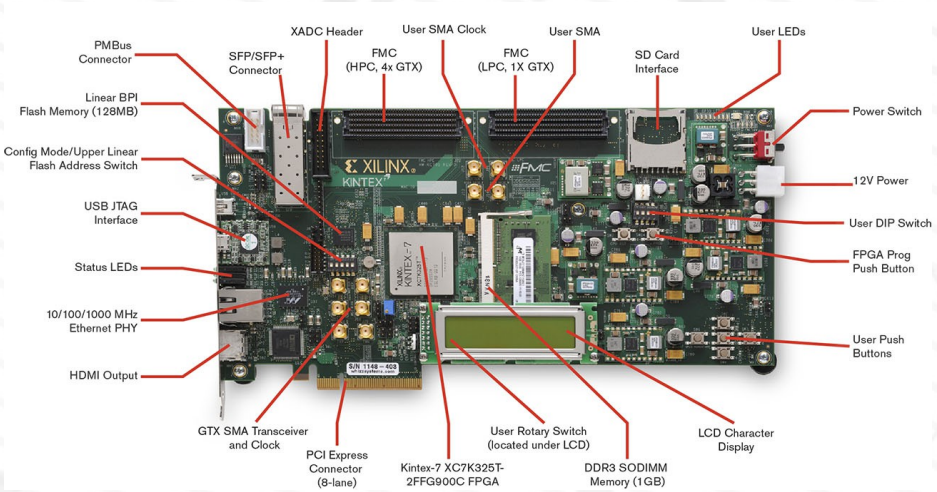


Implement an error rate test system to check the data using a receiver similar to MuCTPiToTopo interface

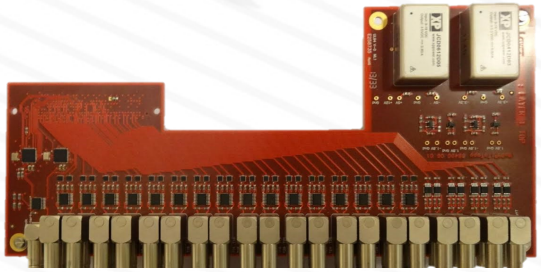
1) Generates a phase scan
2) Calculate Bit Error Rate (BER)

Test system hardware platform

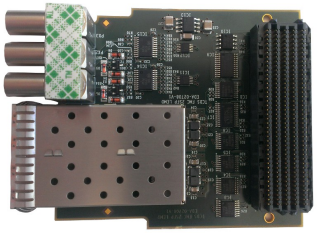
- Xilinx Kintex-7 FPGA ev. board
  - FPGA equipped with programmable internal delay lines
  - Gigabit Ethernet interface
  - High-speed memory module
  - Connectivity to two FMCs



- MUCTPI receiver mezzanine card
  - 32 inputs and 8 outputs
  - NIM to LVDS or LVDS to NIM level converters
  - Jitter-cleaner with input to output phase skew uncontrolled

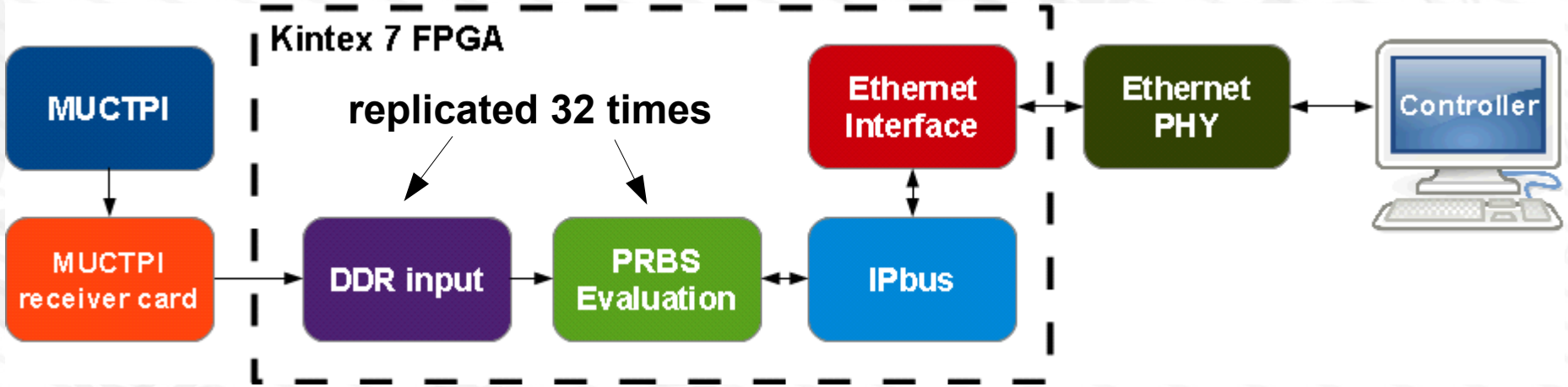


- ECL-LVDS level converter mezzanine card
  - Level converter with constant delay



Test system firmware

- Firmware block diagram



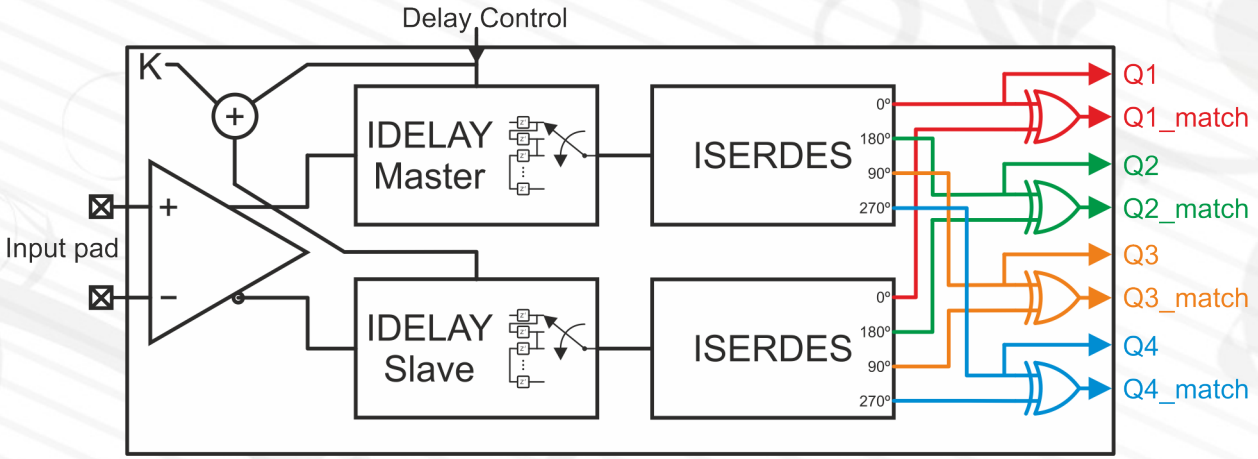
Adjust the phase and detect transitions

Monitor transitions and count bit errors

Control the hardware based on requests from the controller

Implement the MAC layer and PHY interface using Xilinx IP cores

DDR input

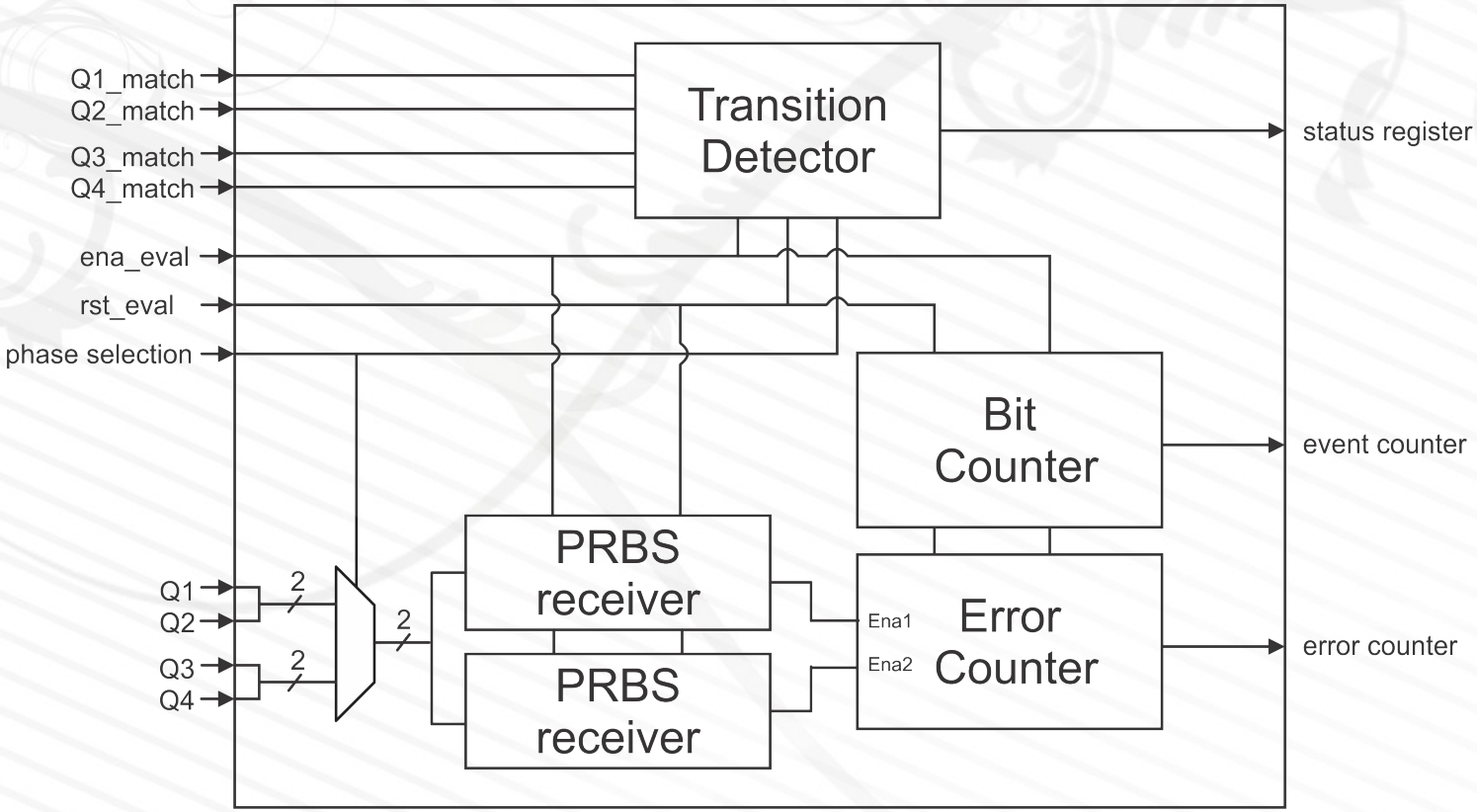


- The delay offset between master and slave paths is always 78.125 ps
- XOR gates are used to compare the data from both paths in order to detect transitions

PRBS evaluation circuit

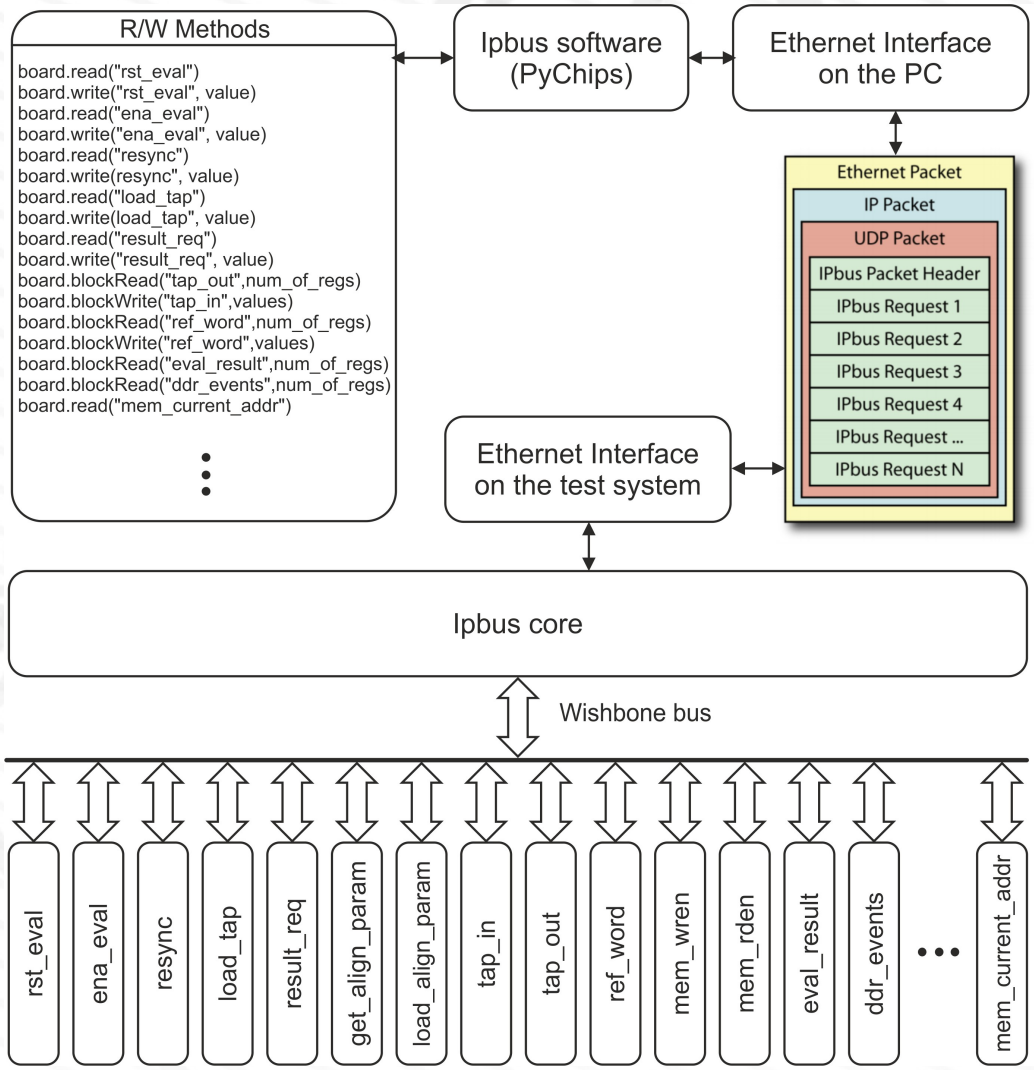
1) Check the existence of transition at a given sampling phase

2) Compare the received PRBS data to a reference and count the number of errors



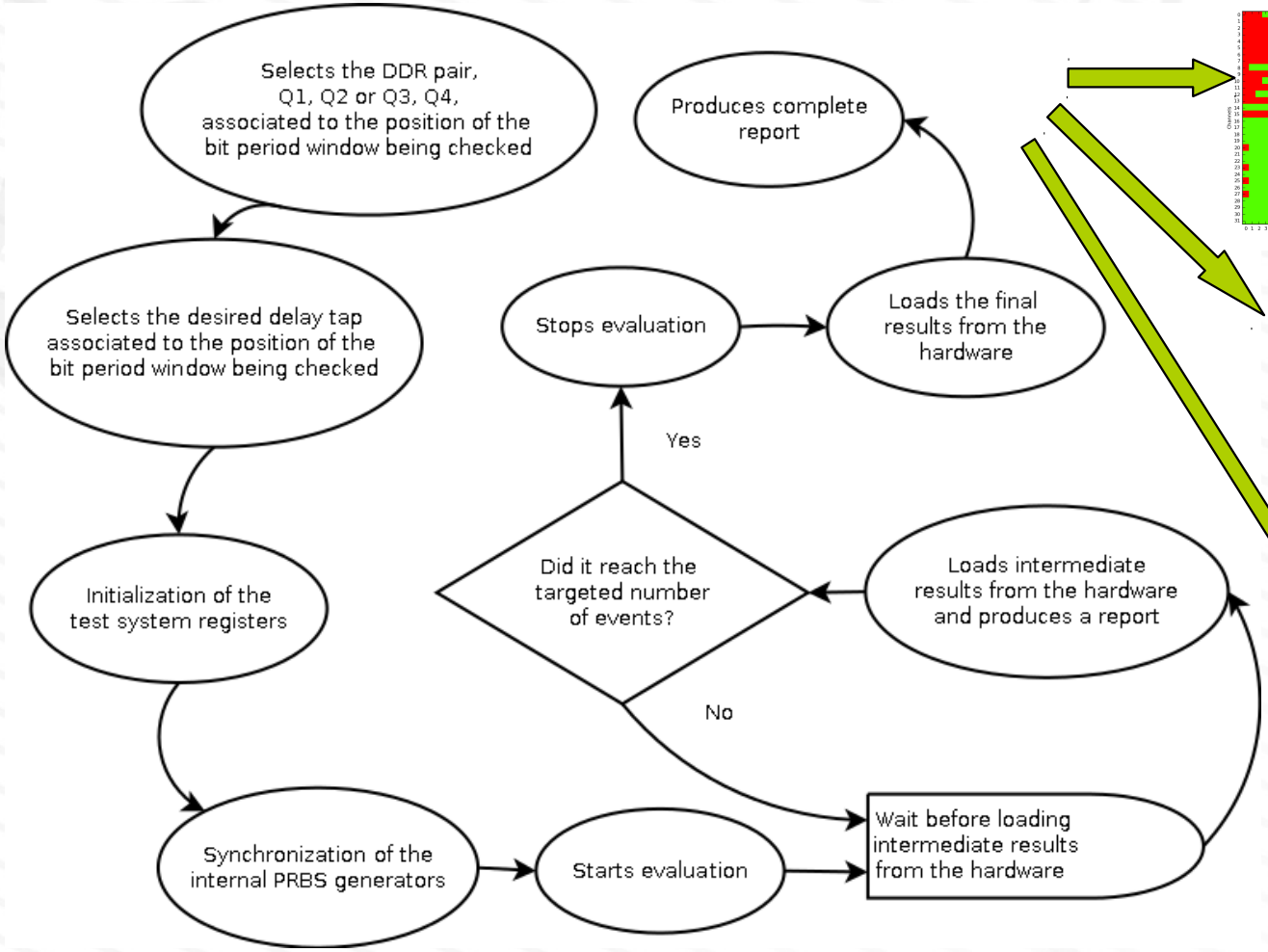
IPbus

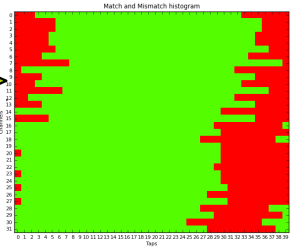
- Configures the DDR input and the transition detector circuit
- Reads out test results through Ethernet
  - PyChips software provides methods to perform R/W requests to registers mapped into a virtual memory space
  - Requests are encapsulated into an Ethernet packet and transmitted through Ethernet
  - At the test system, the IPbus core decodes the packet into R/W bus transactions requests based on the Wishbone standard

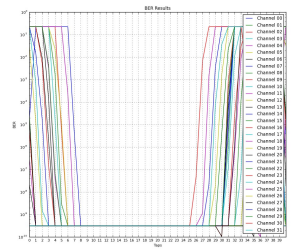


Test system software

- Software written in Python scripting language
- Control and reads out results from the test system generating:





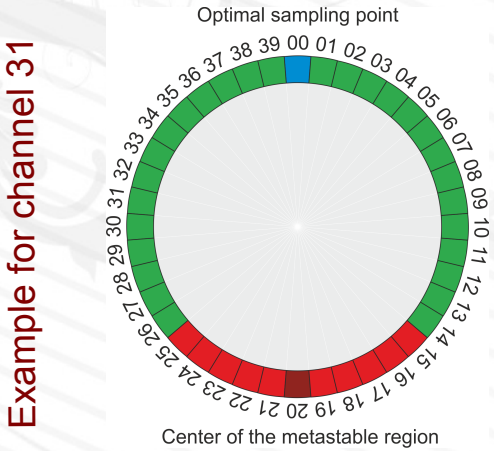


Taps	Channel 00 Errors	Channel 00 Events	Channel 00 BER	Channel 01 Errors	Channel 01 Events	Channel 01 BER
00	160382702	320710744	5.00085e-01	160382702	320710744	5.00085e-01
01	160453066	320852190	5.00084e-01	160453066	320852190	5.00084e-01
02	160350960	320647438	5.00085e-01	160350960	320647438	5.00085e-01
03	160332272	320609838	5.00085e-01	160332272	320609838	5.00085e-01
04	160391364	320728204	5.00085e-01	160391364	320728204	5.00085e-01
05	160432752	320811246	5.00085e-01	160432752	320811246	5.00085e-01

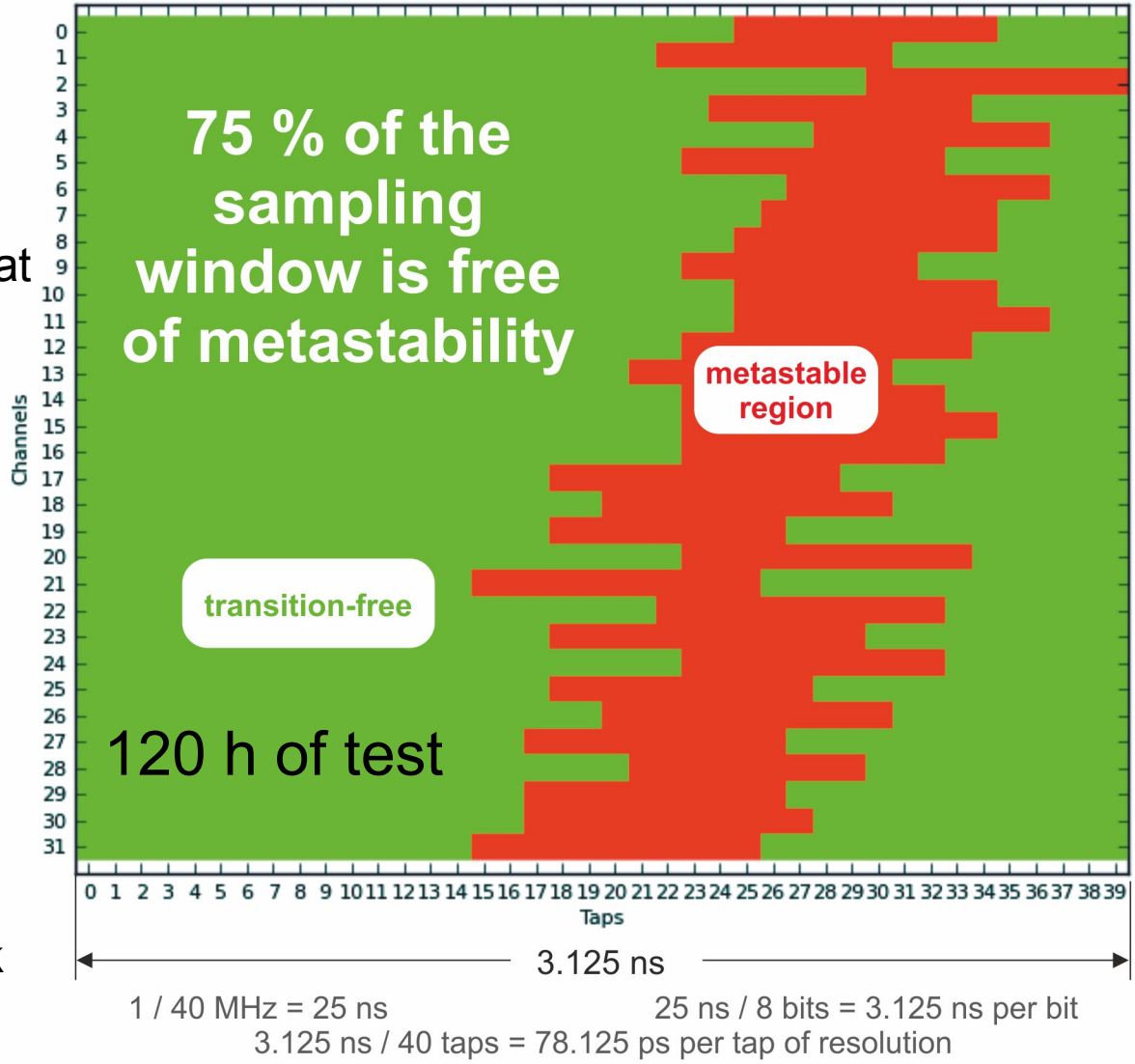
```
prbs_eval - INFO - ########################
prbs_eval - INFO - # Loading the tap: 00. #
prbs_eval - INFO - ########################
prbs_eval - INFO - Loading taps.
prbs_eval - INFO - Innitializing registers.
prbs_eval - INFO - Resetting evaluation.
prbs_eval - INFO - Synchronization request.
prbs_eval - INFO - Activating the evaluation.
prbs_eval - INFO - Wainting for 0.1 seconds until request the results.
prbs_eval - INFO - Desactivating the evaluation.
prbs_eval - INFO - Printing the results.
prbs_eval - INFO - CH.: 00    Match: True Errors: 0000000000  Events: 31638256.
prbs_eval - INFO - CH.: 01    Match: True Errors: 0000000000  Events: 31638256.
```

Test system results

- Transition detection
  - Comfortable timing margin
  - Reliable data reception can be achieved sampling data at the optimal sampling point



  - Additional tests of 120 h did not indicate drift of the clock phase longer than 80 ps



Bit error rate results

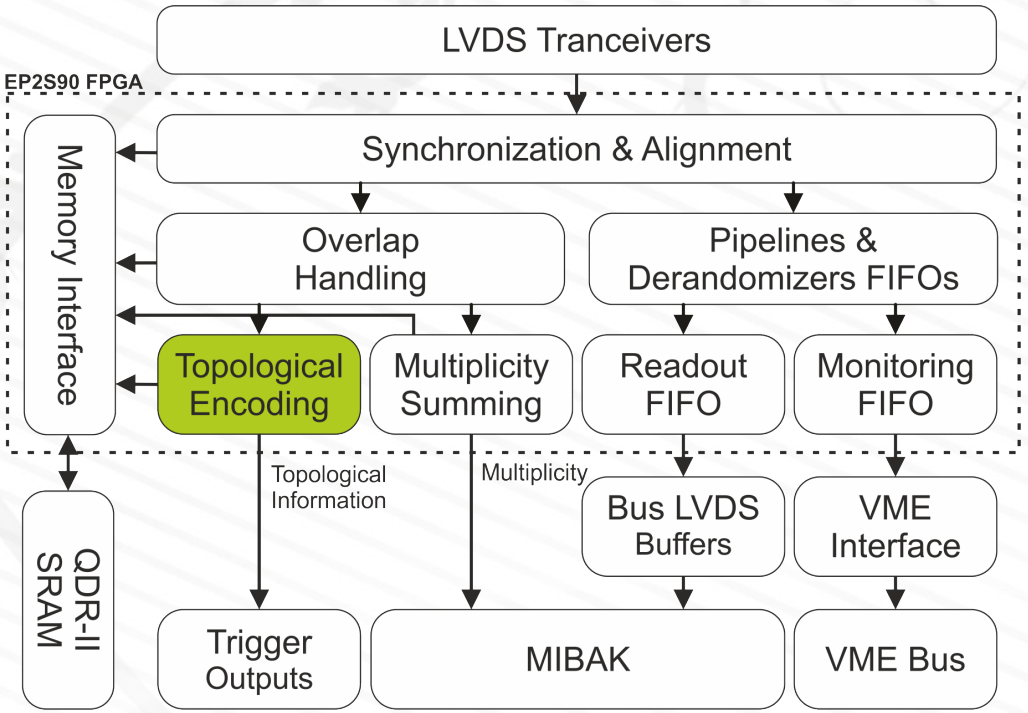
- The probability of error can be estimated to be lower than an upper-limit with a confidence level CL
- The upper limit being 1 x 10^{-15} is equivalent to no errors in the data transmission of the 32 MUCTPI trigger outputs operating at 320 Mbps during 24 h
- After 120 h, 4.42 x 10^{15} bits were transmitted through the electrical trigger outputs without errors.

Therefore, it is estimated that the probability of error in the data transmission using the MUCTPI electrical trigger outputs is lower than the upper-limit of 1 x 10^{-15} (no errors in 24 h) with a confidence level of 98.80 %

MUCTPI upgrade for LHC Run 2

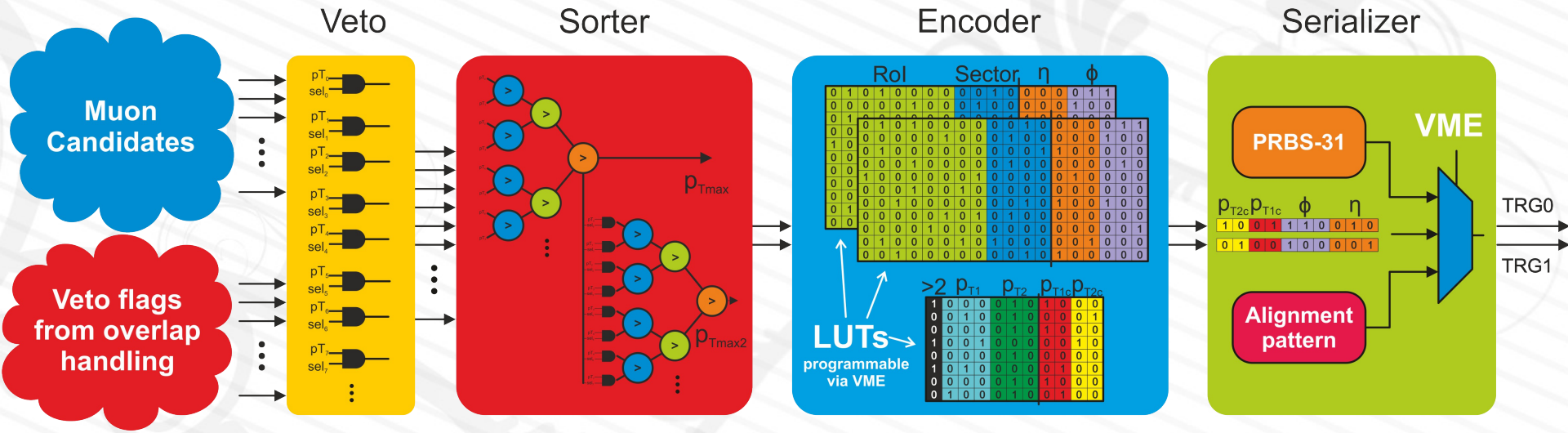
MUCTPI upgrade

- Topological encoding unit was added
  - Extract, encode topological information from the two highest-pT candidates
  - Transmit the data through the electrical trigger outputs at 320 Mbps.
- In addition:
  - Memory interface connections were changed to include debugging information from the topological encoding unit
  - 32-bit monitoring counters to indicate the presence of one, two, or more than two candidates.
  - The topological information is serialized at 320 Mbps using DDR outputs.



MUCTPI upgrade

- Topological Encoding unit block diagram



- The logic of the four stages is clocked at 4 times the BC
- Veto unit
  - Candidates flagged by the overlap handling unit are suppressed
  - The remaining candidates are forwarded to the sorting unit
  - The veto flags registers are duplicated in order to decouple the timing of the multiplicity and topology encoding paths

Sorter unit

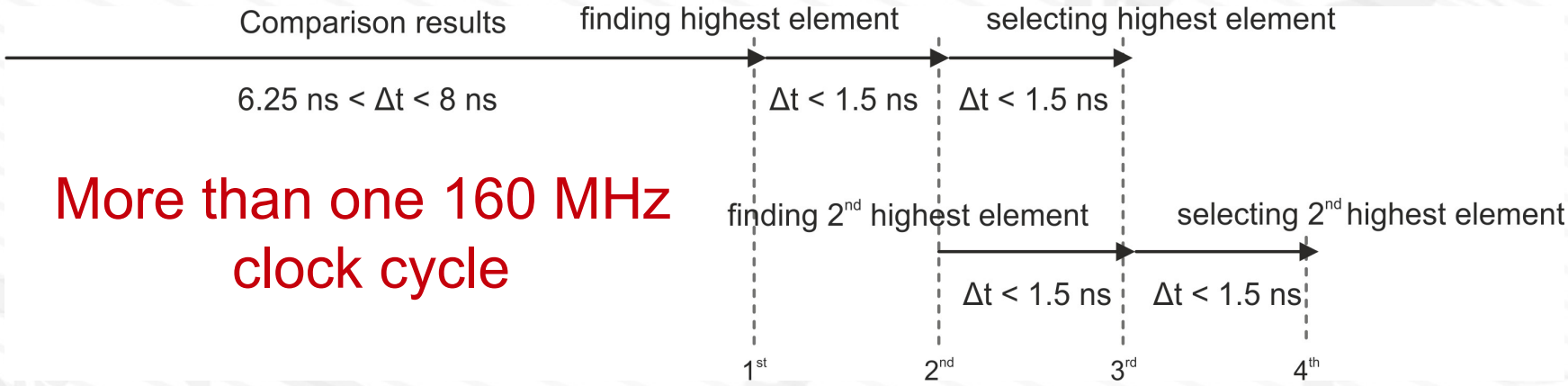
- It sorts the muon candidates according to their pT values and outputs the sector number, RoI and pT value of the 1st and 2nd highest-pT candidates.
- Sequential sorting using one comparator would take 162.5 ns, which is too long when compared to the overall MUCTPI latency of 125 ns
- Therefore a parallel implementation has to be used
- 325 comparisons are used to find the 1st and 2nd highest-pT candidates from a set of 26 candidates

Example for five candidates

	b	**c**	**d**	**e**
a	$p_{Ta} \geq p_{Tb}$	$p_{Ta} \geq p_{Tc}$	$p_{Ta} \geq p_{Td}$	$p_{Ta} \geq p_{Te}$
b	$\overline{(p_{Ta} \geq p_{Tb})}$	$p_{Tb} \geq p_{Tc}$	$p_{Tb} \geq p_{Td}$	$p_{Tb} \geq p_{Te}$
c	$\overline{(p_{Ta} \geq p_{Tc})}$	$\overline{(p_{Tb} \geq p_{Tc})}$	$p_{Tc} \geq p_{Td}$	$p_{Tc} \geq p_{Te}$
d	$\overline{(p_{Ta} \geq p_{Td})}$	$\overline{(p_{Tb} \geq p_{Td})}$	$\overline{(p_{Tc} \geq p_{Td})}$	$p_{Td} \geq p_{Te}$

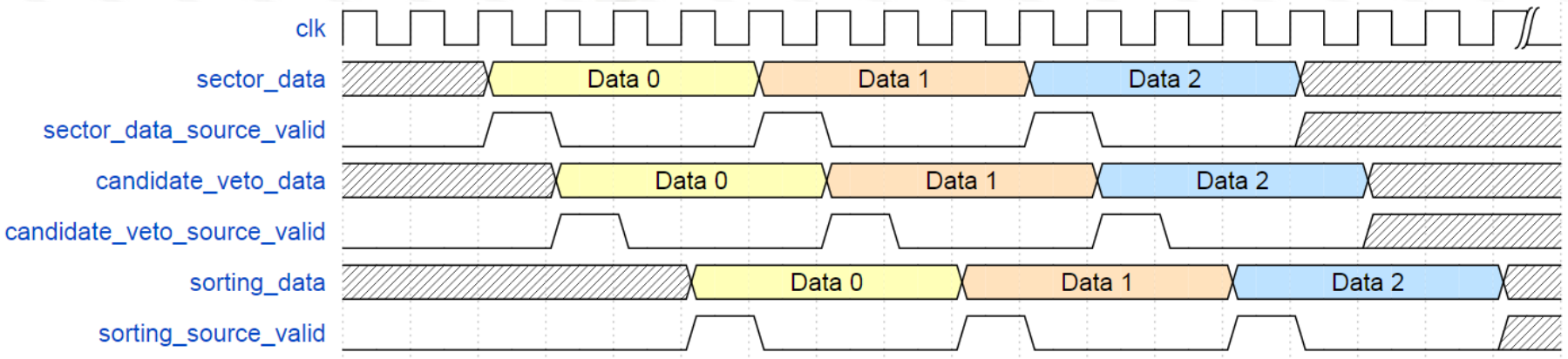
Sorter unit

- Timing diagram



More than one 160 MHz clock cycle

- The acceptable propagation delay for the first stage of the sorting unit was increased to two clock cycles, which was also enough to include the logic from the other three stages into the same path



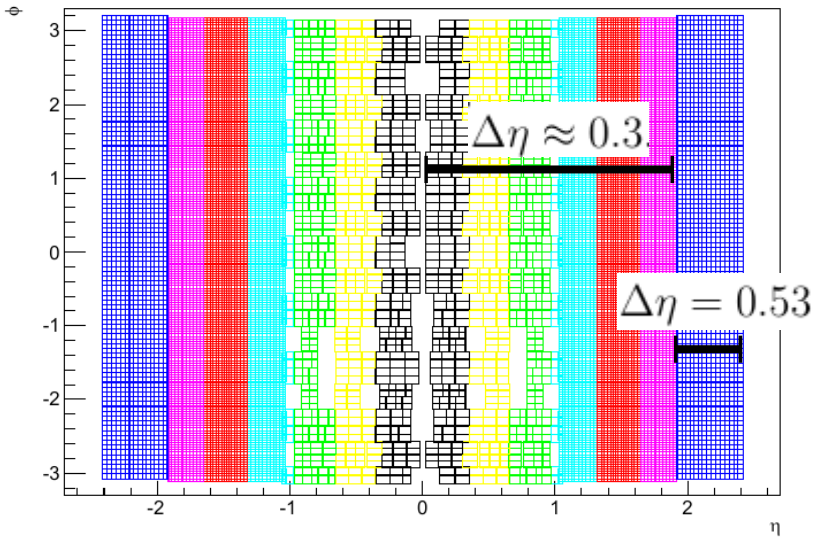
Encoder unit

- The eight bits of topological information were allocated based on a compromise between the available bandwidth, derived from the feasibility test, and the best trigger efficiency from physics simulations

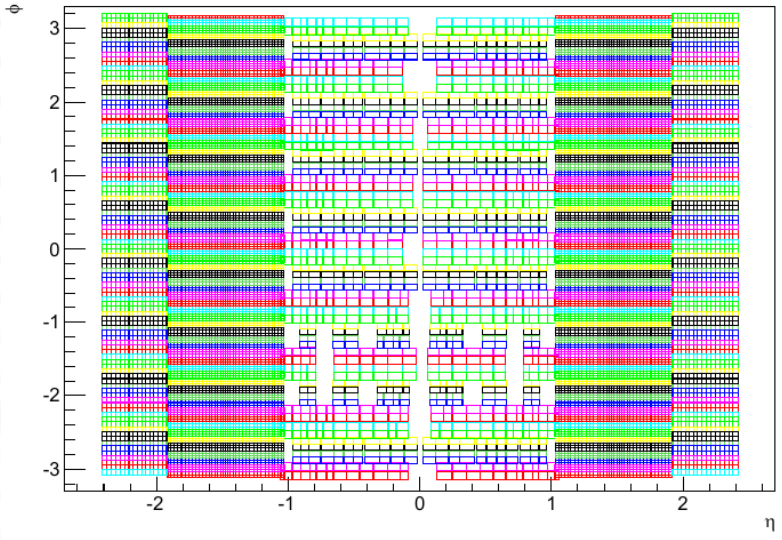
Bit position	7	6	5	4	3	2	1	0
Trigger output	η			ϕ			p_T	

→ $\Delta\eta \times \Delta\phi \approx 0.3 \times 0.1$

Seven codes out of eight are used to encode Eta, the remaining one is used to indicate the absence of any candidate

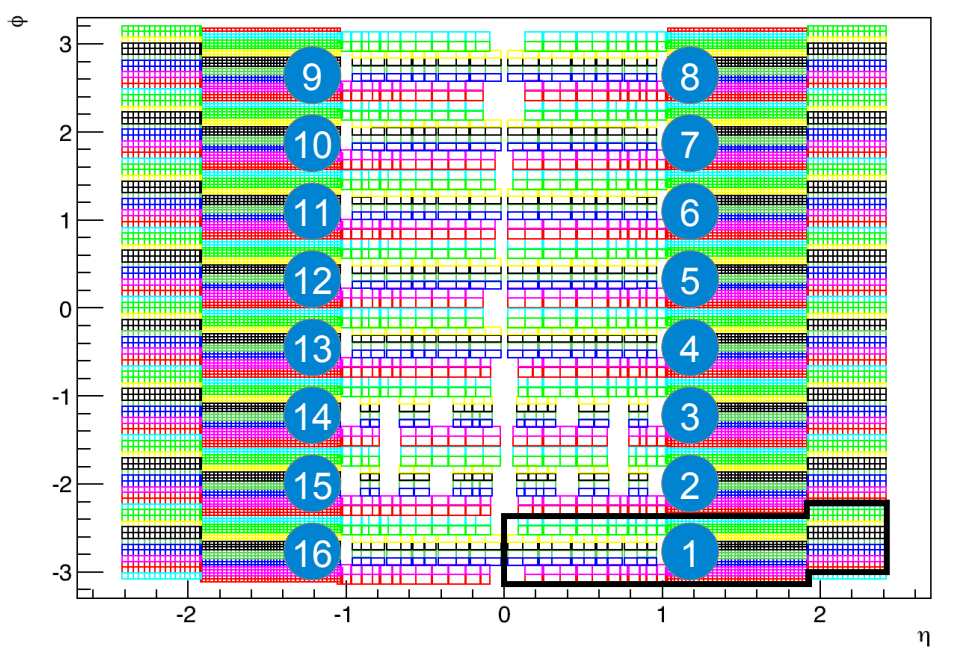


The eight codes are used to encode the Phi information resulting in a unique bin size $\Delta\phi < 0.1$



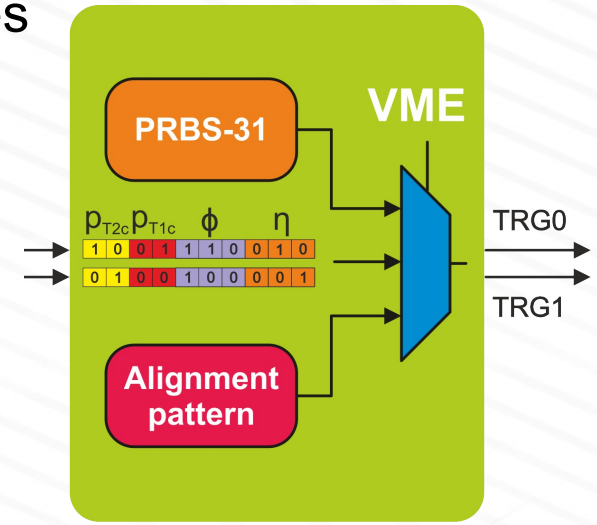
Encoding summary

- Each MIOCT encodes **7 x 8 = 56** geometric locations
- An extended Eta, Phi coordinate is defined using the cable connection information
  - For instance, the octant number and consequently the side (A or C) can be derived from cable connections from MUCTPI and MuCTPiToTopo
- Therefore the MUCTPI system encodes **16 x 56 = 896** geometric locations



Serializer

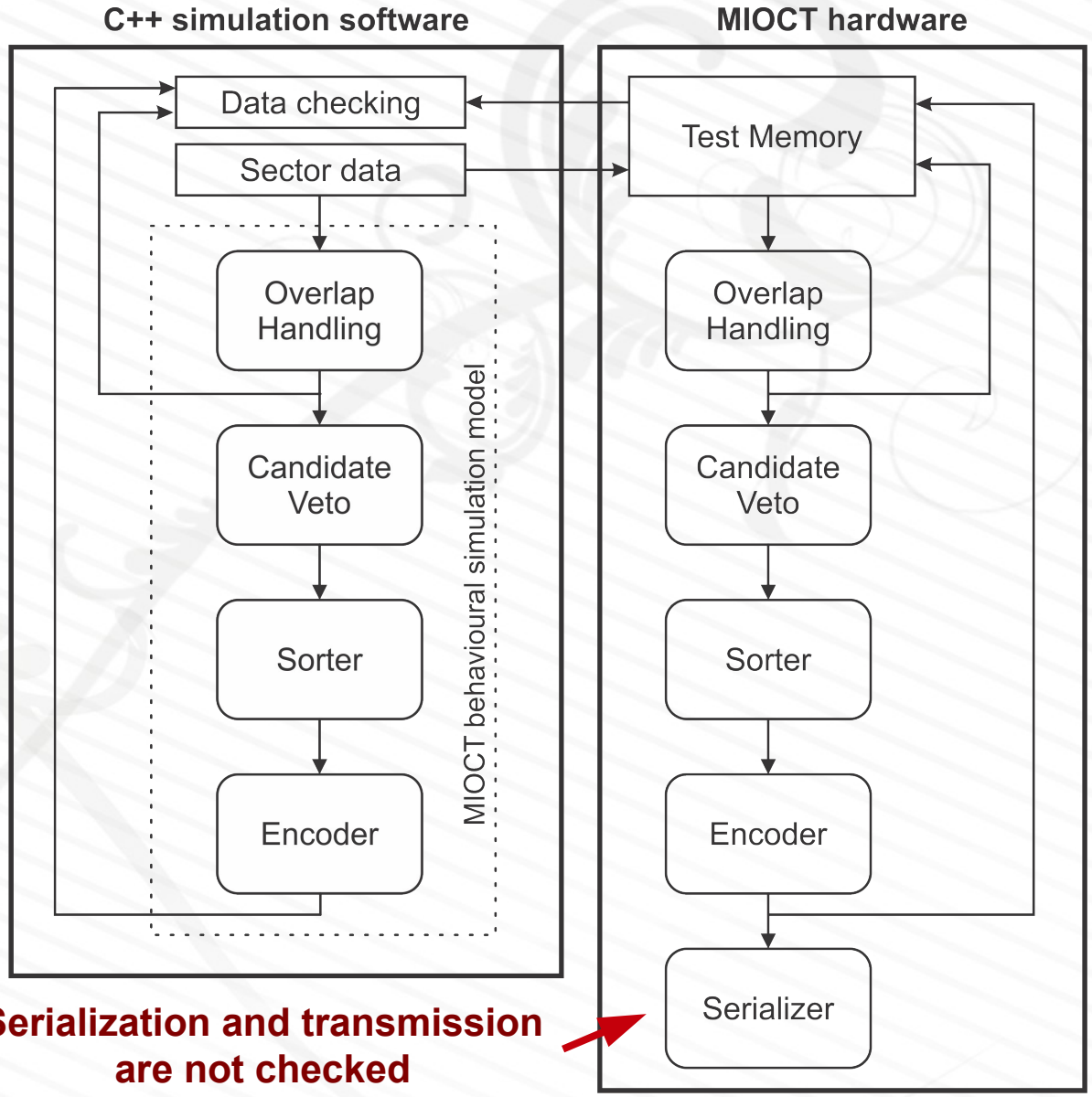
- The 8-bit word is serialized at 320 Mbps and transmitted using DDR outputs
- A separated serializer for each output is implemented using a shift register that first outputs the most significant bit
- The two electrical trigger outputs carry the information from the 1st and 2nd highest-pT candidates respectively
- It can also generate a fixed 16-bit training pattern to be used for phase and word alignment to MuCTPIToTopo
- For test purposes, the serialization unit also features the same PRBS generator used in the feasibility tests



Verification tests of the MUCTPI firmware upgrade

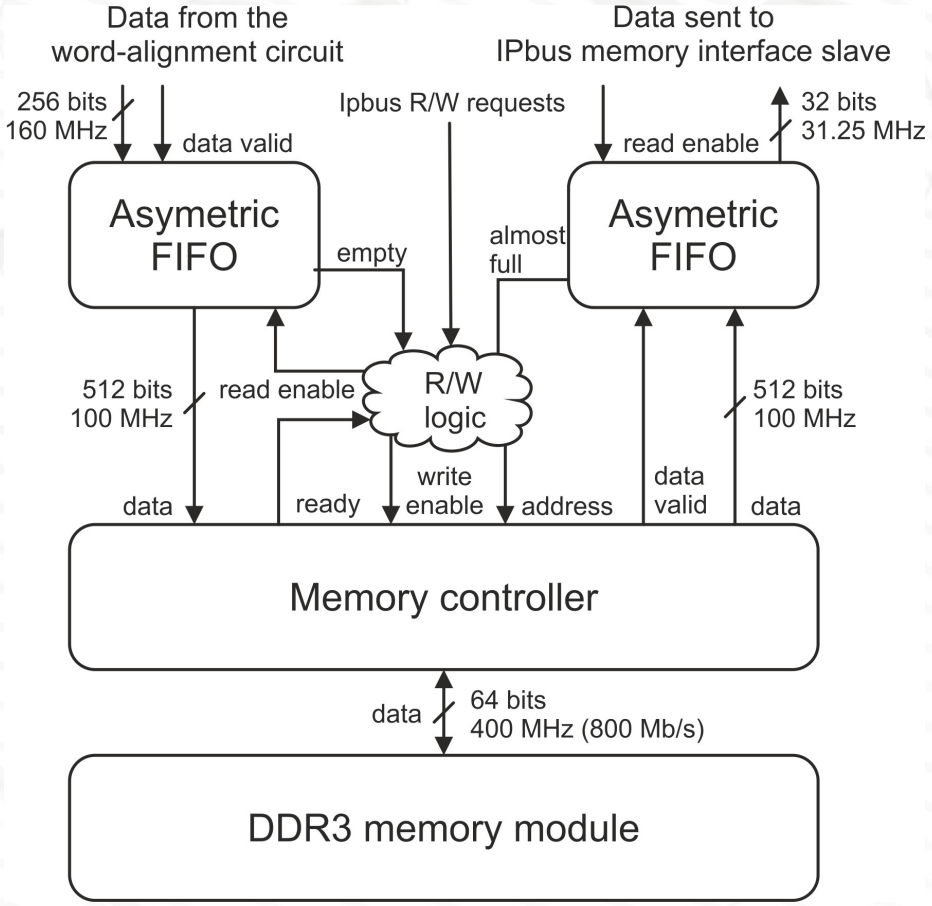
In-system verification

- Checks MIOCT hardware in operation
- Comparing results from the hardware using a software-based reference
- Writes random generated sector data to a test memory, which supplies sector data to the overlap handling unit and reads back the generated veto flags and topology information
- Checked data from approximately 1.4 billions of bunches without errors.



Upgrade of the error rate test system and test result

- The error rate test system was upgraded to receive serialized data from 32 MUCTPI electrical trigger outputs, align them, and write information into a memory module in order to be read out by a computer for verification.
- The word alignment circuit compares input data to predefined 8-bit alignment reference value.
- The Memory interface receives the information from 32 channels, groups it in 512-bit words and writes them to the external memory module
- Checked data from approximately 1 x 10^{10} bunches without errors.



Summary of the Verification tests

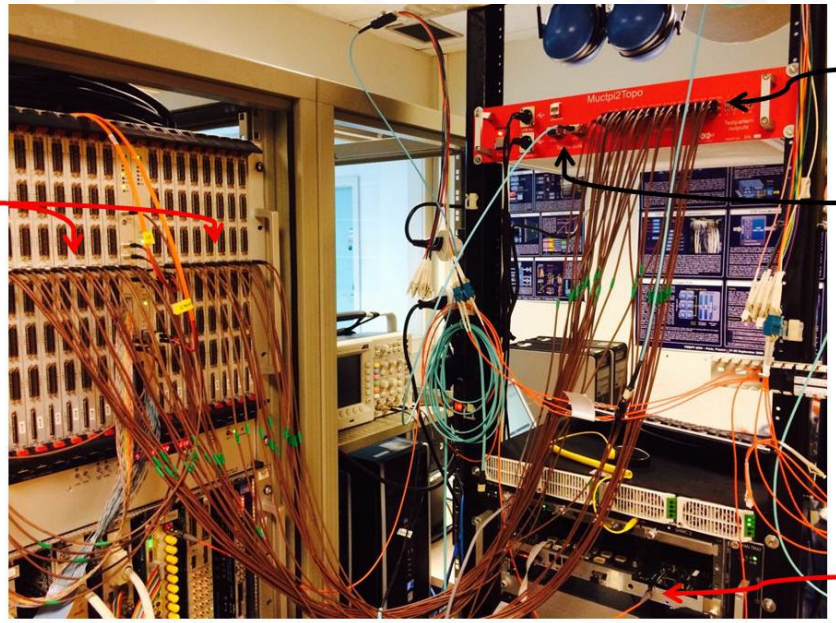
- Functional Simulation: No errors in 185 thousand test patterns
- In-system verification: No errors in 1.4 billion test patterns
- Verification using the test system: No errors in 1×10^{10} test patterns

These results demonstrate that the topological information can be transmitted and received reliably

Integration Tests

Integration tests

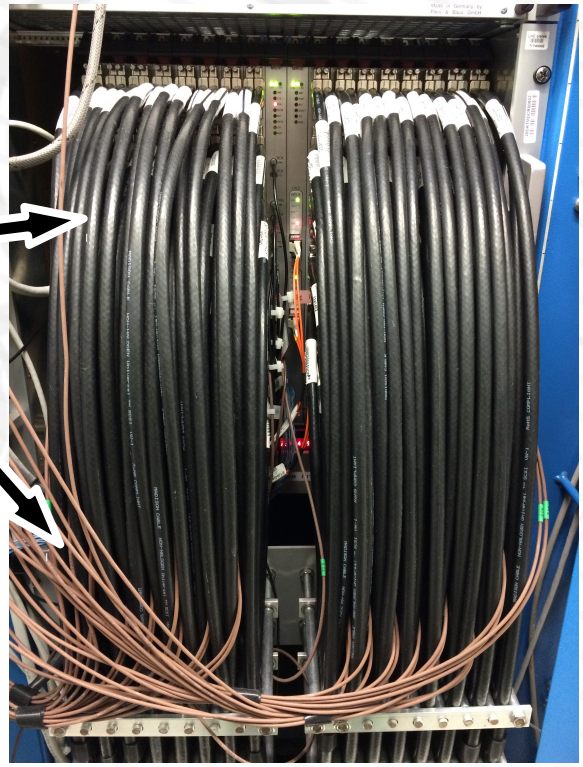
- The **MUCTPI** system was put to integration tests with **MuCTPiToTopo** interface and **L1Topo** in order to verify the interface between the systems.
- The received data by both systems are written to on-chip memories, from where they were read out for verification
- The connectivity test between the MUCTPI system and the MuCTPiToTopo checked data from **2.6 M bunches** in an overnight test. Then, the L1Topo was included in the chain for a second test, which checked **258 k bunches**
- **Both of the tests ran without errors**



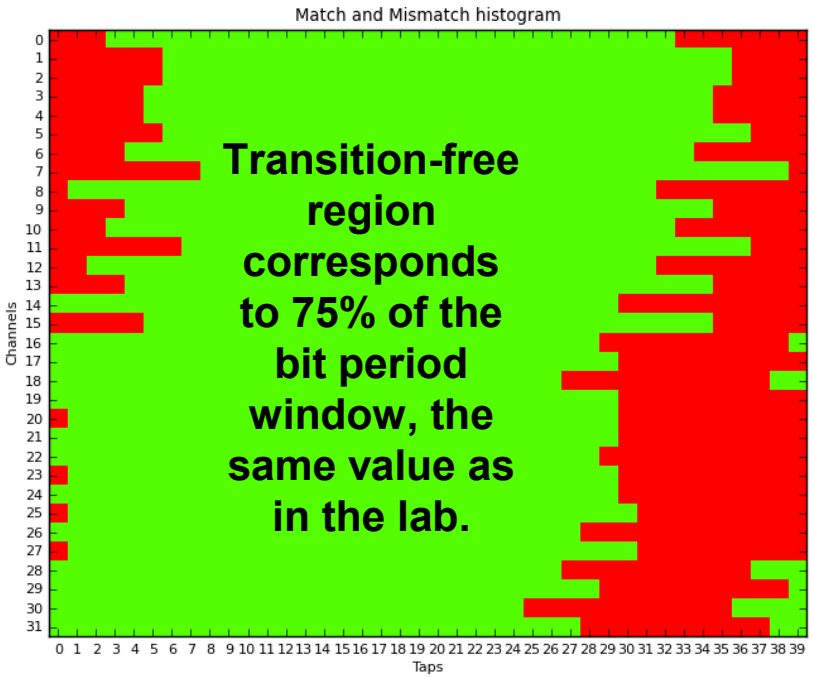
No errors were seen in the data transfer between MUCTPI, MuCTPiToTopo and L1Topo

MUCTPI hardware tests in USA15

- The MUCTPI system installed in USA15 was tested using the error rate test system
  - sector data input from the trigger sector logic
  - trigger output cables connected to the error rate test system



Different phase offset due to the different timing of the system in USA15



The system at USA15 has the same timing margin as the system in the lab

Conclusions

Conclusions

- The MUCTPI firmware was modified to provide muon topological information to L1Topo
- The feasibility using the test system developed demonstrated that the MUCTPI can reliably transmit data to L1Topo using the electrical trigger outputs operating at a bit rate of up to **320 Mbps**
- The BER is estimated to be lower than **1 x 10^{-15} (24 h)** with confidence level of **98.80 %** at the optimal sampling point
- The upgraded MUCTPI was checked by:
  - Computer simulation
  - In-system verification
  - Verification using the upgraded error rate test system
    - In this step, the serialization and transmission of topological information were also checked
- No errors were seen in the interface between MUCTPI, MuCTPiToTopo, and L1Topo in the integrations test

Conclusions

- A test of the electrical trigger outputs of the MUCTPI system in USA15 was performed using the test system. The same timing margin was found when compared to the system in the laboratory
- The results demonstrated that the system installed is ready for commissioning tests

- Next steps:
  - Commissioning of the system in USA15 once L1Topo and MuCTPiToTopo interface are ready for integration
  - Documentation

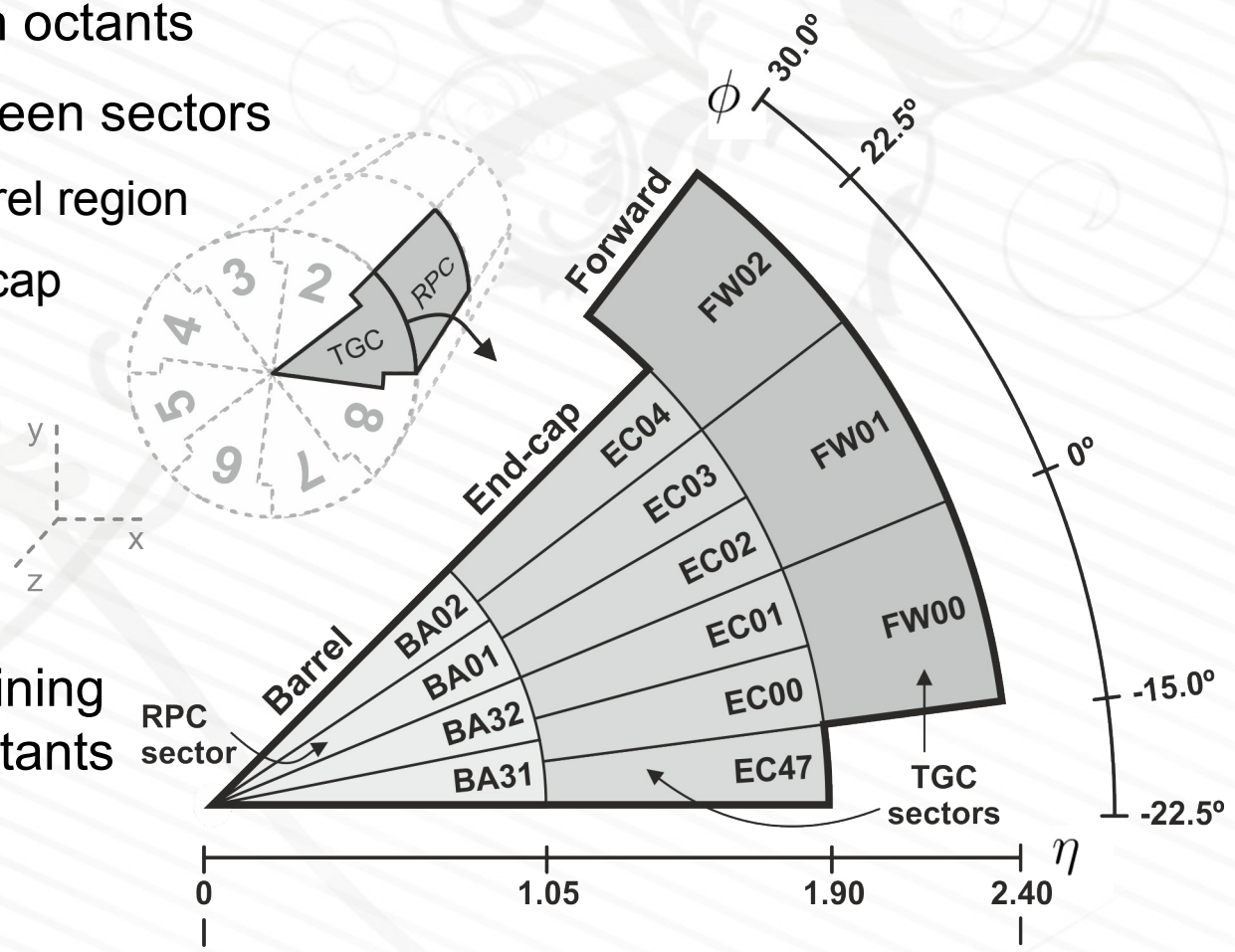
Acknowledgements

- I would like to thank my supervisors Stefan Haas and Augusto Santiago
- I am also grateful for the support from UFJF, CERN and CAPES
- I would like to acknowledge with gratitude my officemates Manoel Barros, Marco Ghibaudi and Dimitrios Kolotouros

BACKUP

Muon trigger detectors segmentation for the MUCTPI

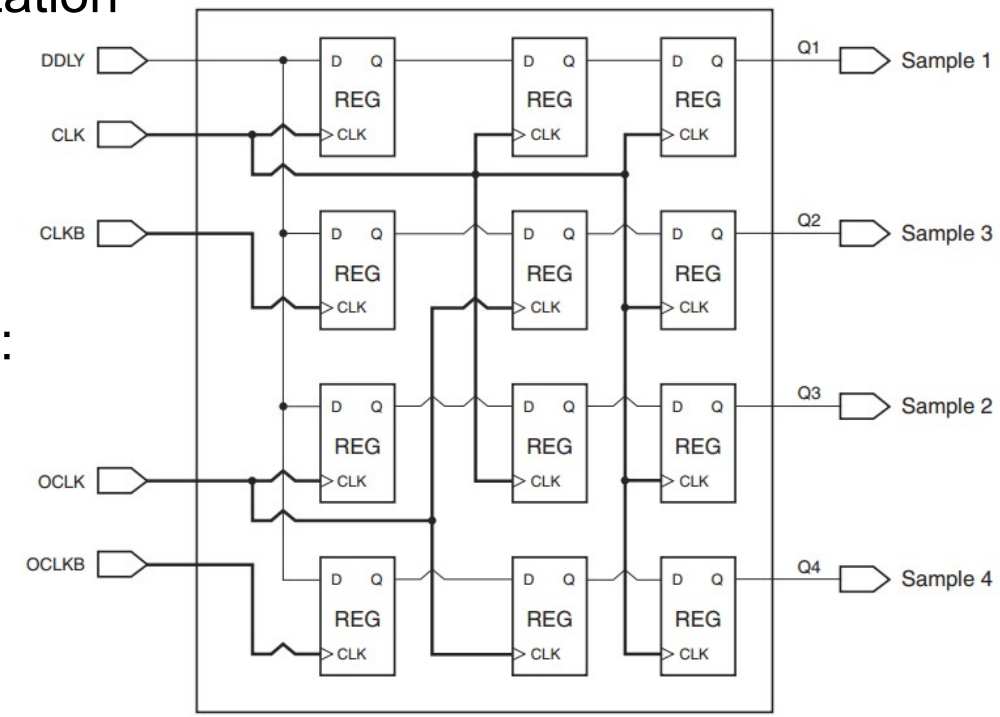
- The muon trigger system is segmented in two halves
- Each half is segmented in octants
- Each octant contains thirteen sectors
  - Four sectors from the barrel region
  - Six sectors from the end-cap region
  - Three sectors from the forward region
- The **MUCTPI** generates the total multiplicity combining the results from the 16 octants



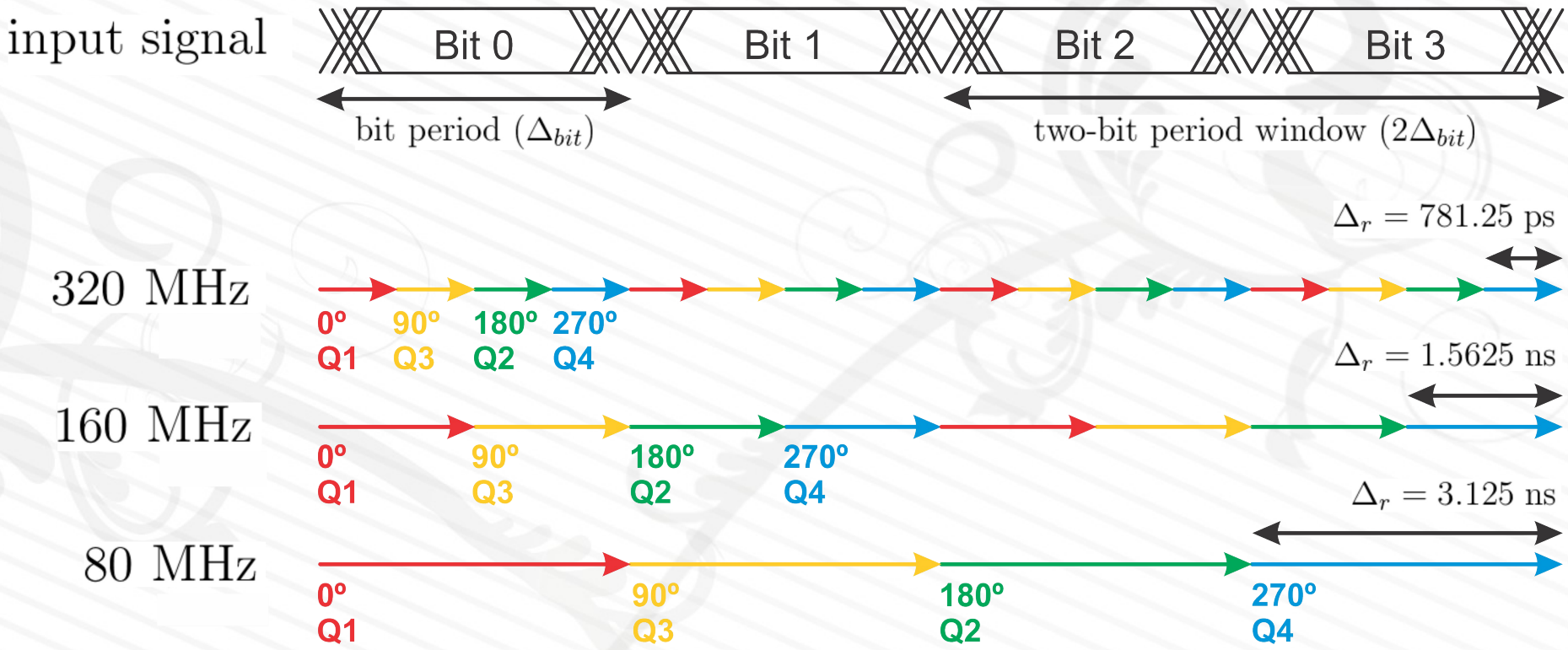
DDR input

- The programmable delay lines offer a maximum delay of 2.5 ns using selectable taps at intervals $\Delta_t = 78.125\,\mathrm{ps}$
- However, the bit period is 3.125 ns in 320 Mbps
- Therefore oversampling the input data is necessary
- Internal serialization and deserialization blocks are used to sample the data at four different positions using four orthogonal clocks (90º phase-shifted)
- Now the delay required is given by:
  - Fclk represents the receiver clock frequency used to sample the data

$$\Delta_r = \frac{1}{4F_{clk}},$$



DDR input

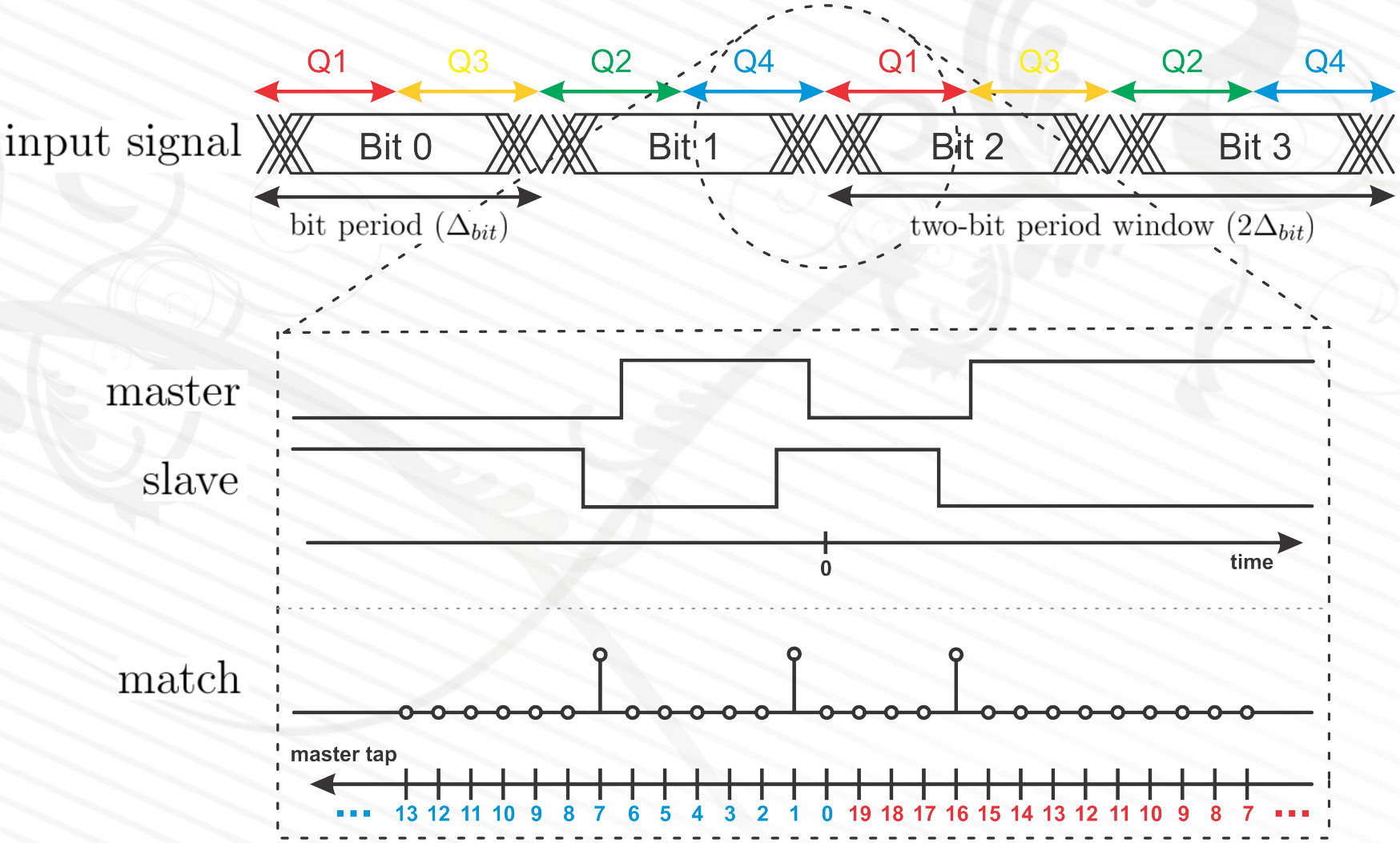


- Oversampling allows the receiver to run at 320 MHz or 160 MHz
- 160 MHz is selected because it simplifies the timing of the system
- The tap selection has to be limited in order to avoid overlap between the four segments of the sampling window

DDR input

$$N_{tmax} = \frac{\Delta_r}{\Delta_t} = \frac{1.5625\,\mathrm{ns}}{78.125\,\mathrm{ps}} \triangleq 20.$$

DDR input

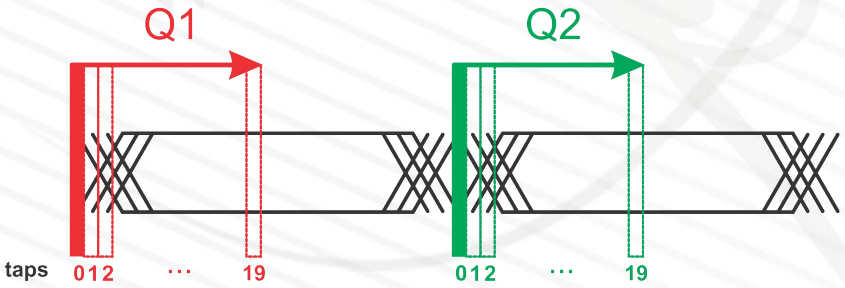

Q1
Q3
Q2
Q4
Q1
Q3
Q2
Q4
input signal
Bit 0
Bit 1
Bit 2
Bit 3
bit period (Δ_{bit})
two-bit period window ($2\Delta_{bit}$)
master
slave
0
time
match
master tap
13 12 11 10 9 8 7 6 5 4 3 2 1 0 19 18 17 16 15 14 13 12 11 10 9 8 7

DDR input

- Measurement is divided into steps
- Each step monitors two match ports simultaneously
- The steps are grouped in two stages
  - First 20 steps Q1 and Q2 are monitored, then Q3 and Q4.

Stage I

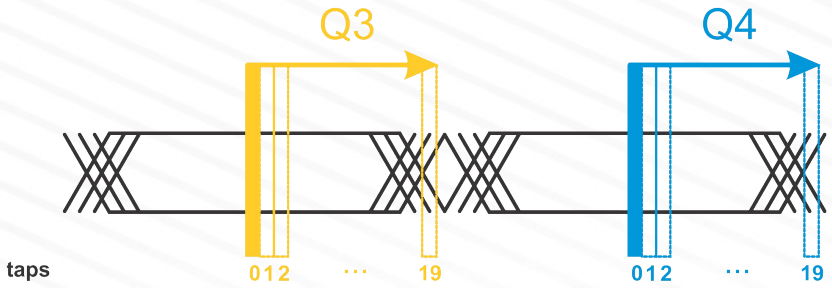
Steps from 0 to 19
Positions from 0 to 19 and 40 to 59



The first and third quarters of the sampling window are checked

Stage II

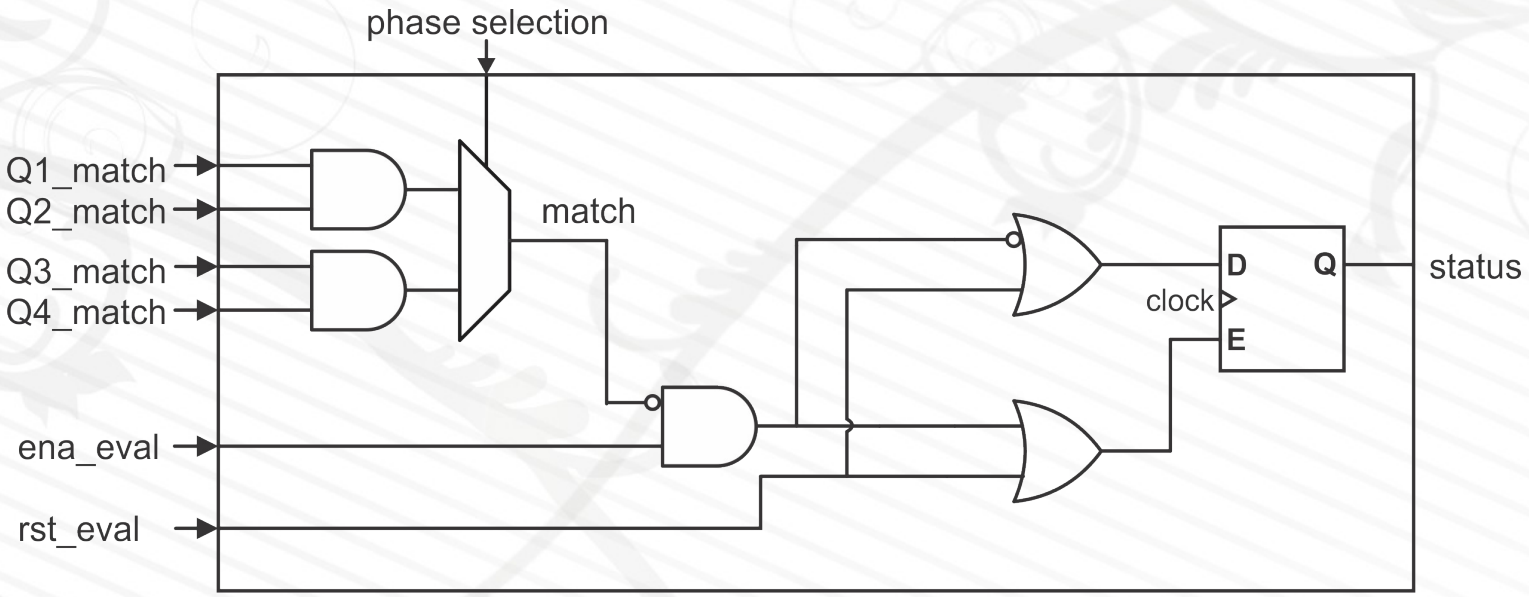
Steps from 20 to 39
Positions from 20 to 39 and 60 to 79



The second and fourth quarters of the sampling window are checked

PRBS evaluation

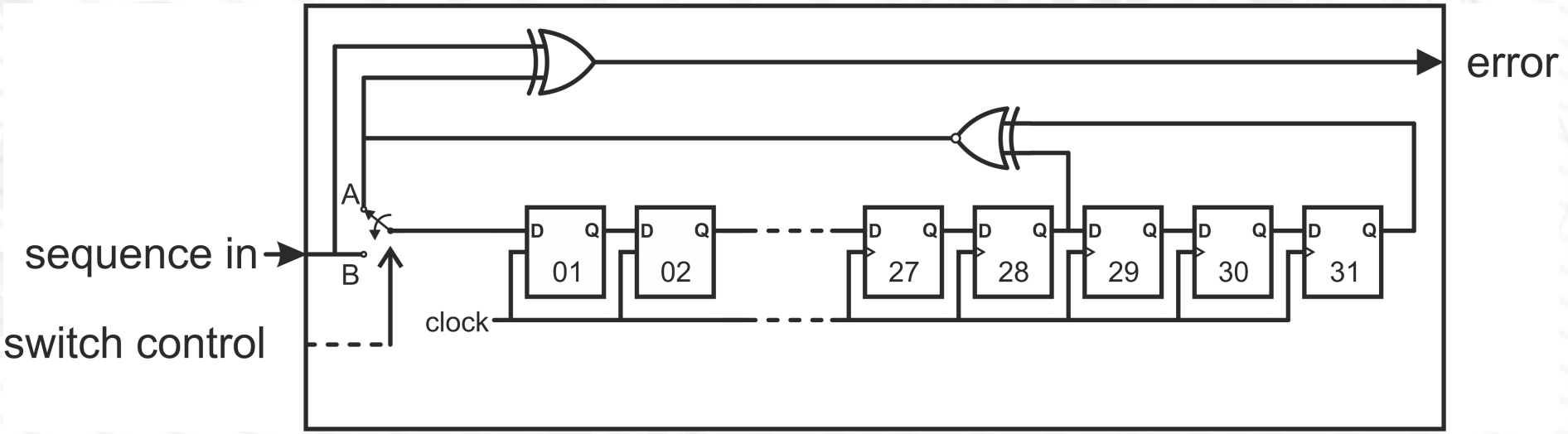
Transition detection circuit



The status is generated by latching the match signal low in a register

PRBS receiver

- Compares the input data to an internally generated pseudo-random sequence



- B: Register are loaded with the input data
  - Loading the 31 registers takes less than 100 ns
- A: Feedback path is connected
  - Generates a free running sequence synchronized with the input pattern

Sorter unit

- The second highest-pT candidate is found inverting the comparison results involving the highest-pT candidate in a second matrix
- Example: the element a is the highest candidate

	b	c	d	e
a	$p_{Ta} \geq p_{Tb}$	$p_{Ta} \geq p_{Tc}$	$p_{Ta} \geq p_{Td}$	$p_{Ta} \geq p_{Te}$
b	$\overline{(p_{Ta} \geq p_{Tb})}$	$p_{Tb} \geq p_{Tc}$	$p_{Tb} \geq p_{Td}$	$p_{Tb} \geq p_{Te}$
c	$\overline{(p_{Ta} \geq p_{Tc})}$	$\overline{(p_{Tb} \geq p_{Tc})}$	$p_{Tc} \geq p_{Td}$	$p_{Tc} \geq p_{Te}$
d	$\overline{(p_{Ta} \geq p_{Td})}$	$\overline{(p_{Tb} \geq p_{Td})}$	$\overline{(p_{Tc} \geq p_{Td})}$	$p_{Td} \geq p_{Te}$

Inverted comparisons

Transverse momentum encoding

- Two bits are used to encode the pT threshold, three of four codes are used to map the original six pT thresholds onto three programmable pT threshold values

	First candidate	Second candidate
00	p_{T_I}	p_{T_I}
01	$p_{T_{II}}$	$p_{T_{II}}$
10	$p_{T_{III}}$	$p_{T_{III}}$
11	not used	more than two candidates

VHDL functional simulation

- The VHDL functional simulation test bench consists of:
  - A VHDL behavioural reference model
  - A VHDL code of the firmware
- The results of the firmware simulation are compared to the reference response
- The veto flags and the four stages of the topological encoding units are checked individually
- The VHDL firmware code was verified by functional simulation using sector data information from approximately 185 k bunches without errors.